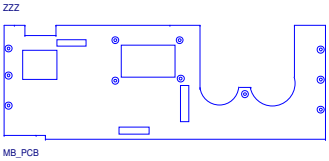


MODEL NAME : ZZZZZZ

PCB NO : LA-E672P

BOM P/N : 43xxxx



Dell/Compal Confidential

Schematic Document

Italia WHL

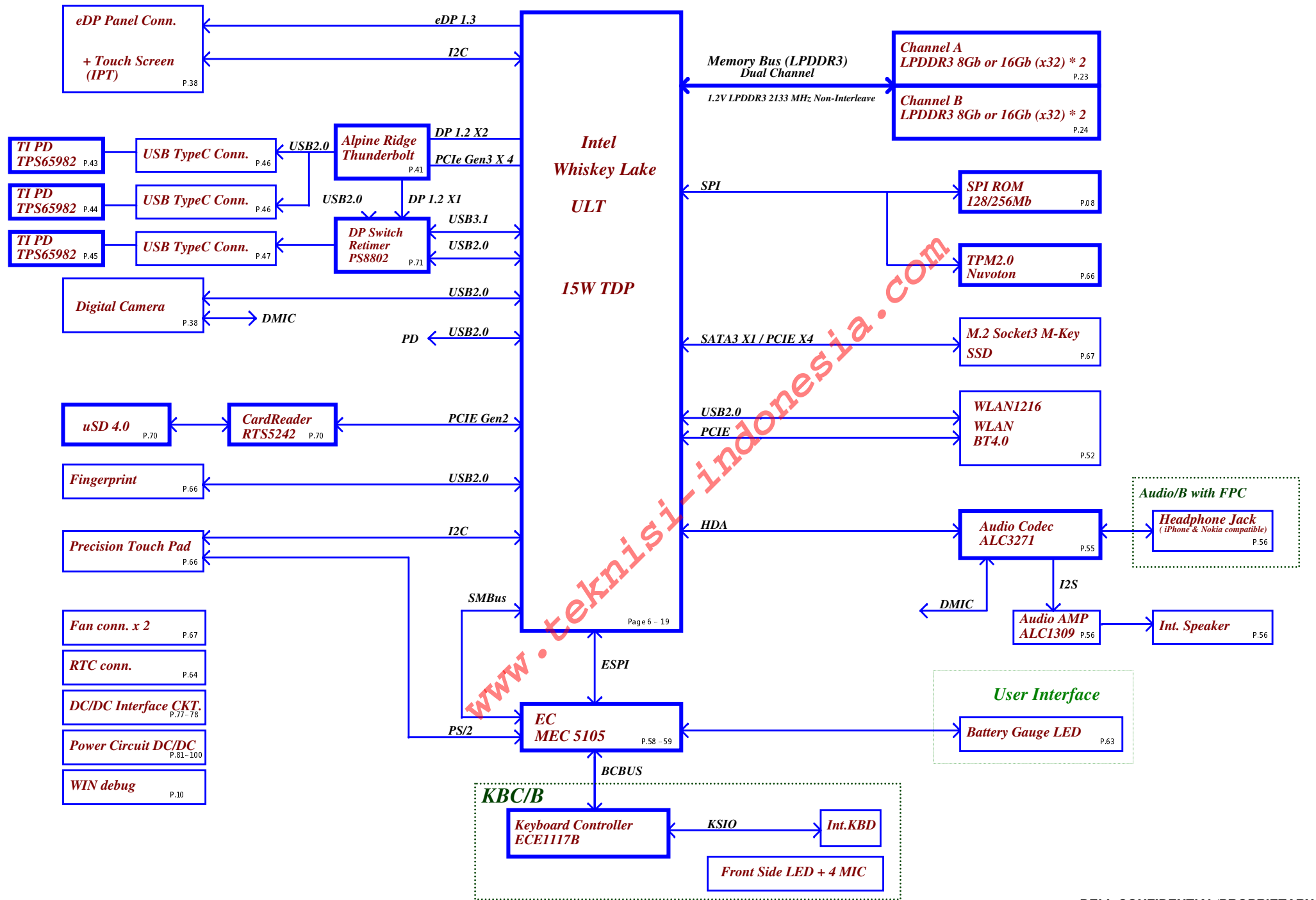
@ : Nopop Component
L@: Intel 8265
XPS@ : Killer1435-S
DCI@ : for DCI Debug
DEBUG@ : for Other Debug
@CONN@ : Reserve Connector Component
@EMC@ : Reserve EMC Component
CONN@ : Connector Component
EMC@ : EMC Component
RF@ : RF Solution Component
XDP@ : XDP Debug Component
RTD3@ : for TBT RTD3 and follow Merion
@RTD3@ : No TBT RTD3

2018-10-22

Rev: 1.0 (A00)

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| | | | | | |
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| Issued Date | 2016/12/16 | Deciphered Date | 2016/12/13 | P01-Cover Page | |
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| | | | | Document Number | 0.1 |
| | | | | LA-E672 | |
| | | | | Date: Tuesday, October 30, 2018 | Sheet 1 of 100 |



Board ID Table for AD channel

| RE194 | CE75 | REV |
|-------|-------|-----|
| 240K | 4700p | X00 |
| 130K | 4700p | X01 |
| 62K | 4700p | X02 |
| 33K | 4700p | X03 |
| 8.2K | 4700p | A00 |
| 4.3K | 4700p | |
| 2K | 4700p | |
| 1K | 4700p | |

| CPU | 4+2 | 2+2 | VPro |
|------------------|-----|-----|------|
| Italia WHL EDO30 | | | |

BOARD_ID rise time is measured from 5%~68%.

SMBUS Control Table

| | SOURCE | BATTERY Charger | PD1 | PD2 | PWR_MON | 5105 | XDP | Audio AMP | eDP | Touch Pad | Touch S | IR_THER_S |
|-----------------------------|---------|--------------------|-----|-----|---------|------|-----|--------------|-----|-----------|---------|-----------|
| SMB00_CLK SMB00_DATA | MECS105 | | | V | | | | | | | | |
| SMB01_CLK SMB01_DATA | MECS105 | | | | | | | | | | | V |
| SMB02_CLK SMB02_DATA | MECS105 | | | | | | | | | V | | |
| SMB04_CLK SMB04_DATA | MECS105 | | V | | | | | | | | | |
| SMB05_CLK SMB05_DATA | MECS105 | | | | | | | V | | | | |
| SMB07_CLK SMB07_DATA | MECS105 | | | | V | | | | | | | |
| SMB10_CLK SMB10_DATA | MECS105 | V | | | | | | | | | | |
| PCH_SML1CLK PCH_SML1DATA | PCH | | | | | V | | | | | | |
| SMBCLK SMBDATA | PCH | | | | | | V | | | | | |
| I2C0_CLK I2C0_DATA | PCH | | | | | | | | | | V | |
| I2C1_CLK I2C1_DATA | PCH | | | | | | | | | V | | |
| I2C2_CLK I2C2_DATA | PCH | | | | | | | | V | | | |



| PCH USB 2.0 Port Mapping | USB PORT# | DESTINATION |
|-----------------------------------|-----------|-----------------|
| | 1 | PD PORT3 |
| | 2 | NC |
| | 3 | NC |
| | 4 | NC |
| | 5 | IR Camera & Cam |
| | 6 | USB PD PORT2 |
| | 7 | NGFF WLAN BT |
| | 8 | NC |
| | 9 | USB PD PORT1 |
| | 10 | Fingerprint |
| PCH USB 3.0 Port Mapping | 1 | DP MX (PS8743B) |
| | 2 | |
| | | |

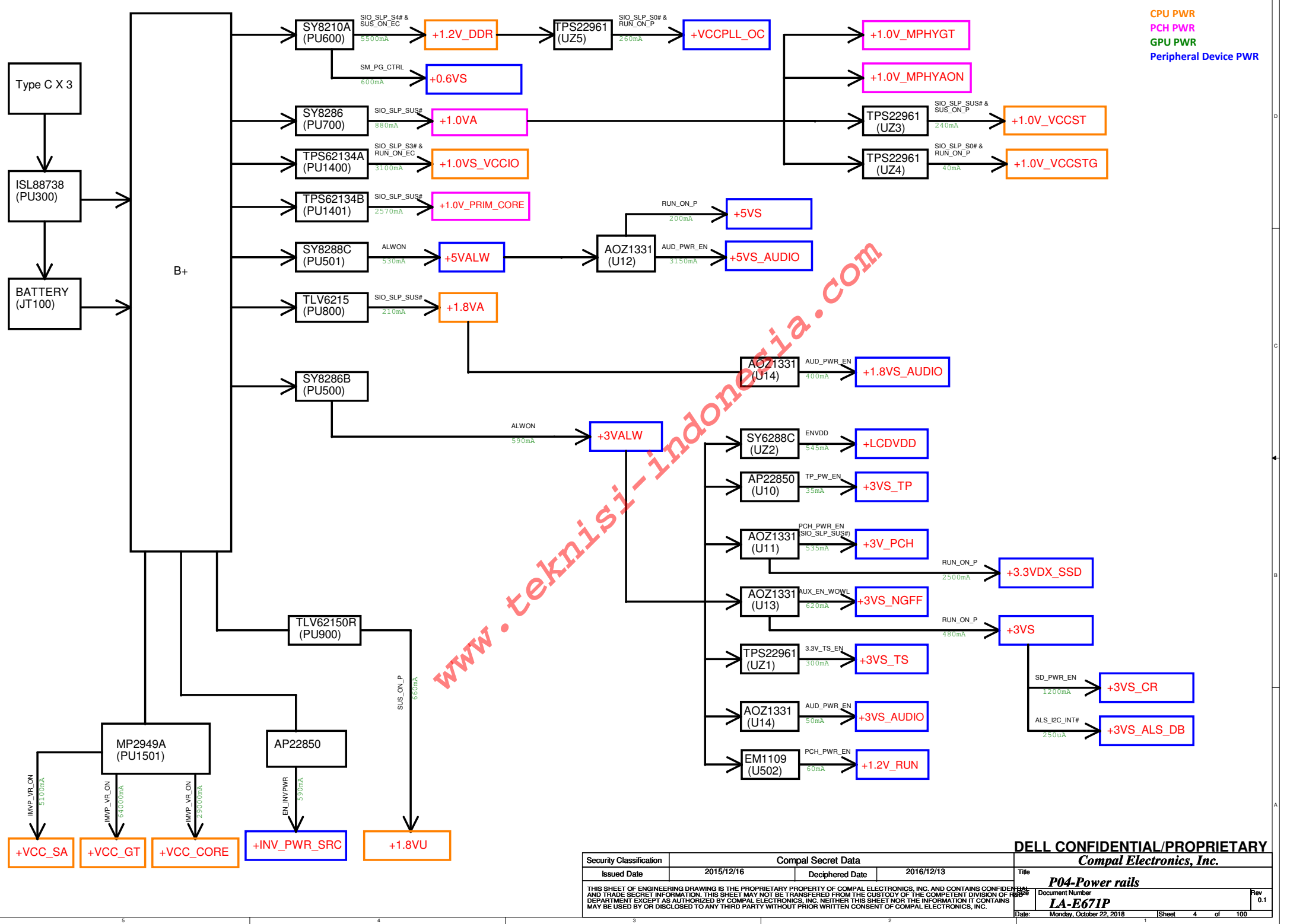
| PCH DDI Port Mapping | DDI PORT# | DESTINATION |
|-------------------------------|-----------|--------------|
| | 1 | Alpine Ridge |
| | 2 | Alpine Ridge |
| | | |

| CLK | DIFFERENTIAL CLK# | DESTINATION | PCI EXPRESS PORT# | DESTINATION |
|-----|-------------------|--------------|-------------------|--------------|
| | CLKOUT_PCIE0 | Alpine Ridge | Lane 5 | Card Reader |
| | CLKOUT_PCIE1 | NGFF WLAN | Lane 6 | NC |
| | CLKOUT_PCIE2 | NC | Lane 7 | NGFF WLAN |
| | CLKOUT_PCIE3 | M.2 SSD | Lane 8 | NC |
| | CLKOUT_PCIE4 | NC | Lane 9 | Alpine Ridge |
| | CLKOUT_PCIE5 | Card Reader | Lane 10 | Alpine Ridge |
| | FLEX CLK# | DESTINATION | Lane 11 | Alpine Ridge |
| | CLKOUT_LPC_0 | ESPI 5105 | Lane 12 | Alpine Ridge |
| | CLKOUT_LPC_1 | NC | Lane 13 | M.2 SSD |
| | CLKOUT_ITPXDP | XDP CONN | Lane 14 | M.2 SSD |
| | | | Lane 15 | M.2 SSD |
| | | | Lane 16 / SATA 2 | M.2 SSD |

| SATA PORT# | DESTINATION |
|------------|-------------|
| SATA-0 | NC |
| SATA-1A | NC |
| SATA-1B | NC |
| SATA-2 | M.2 SSD |
| | |
| | |

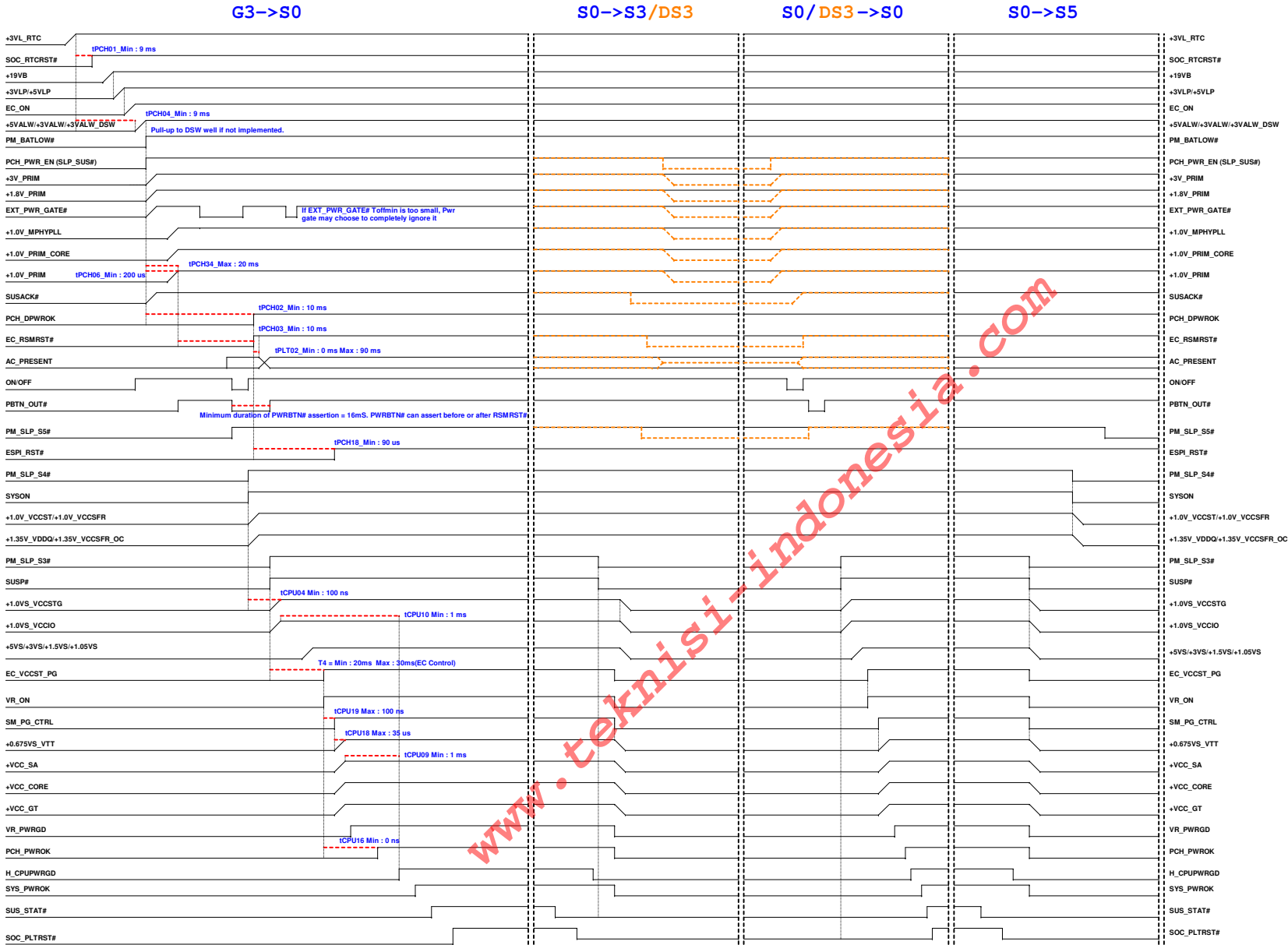
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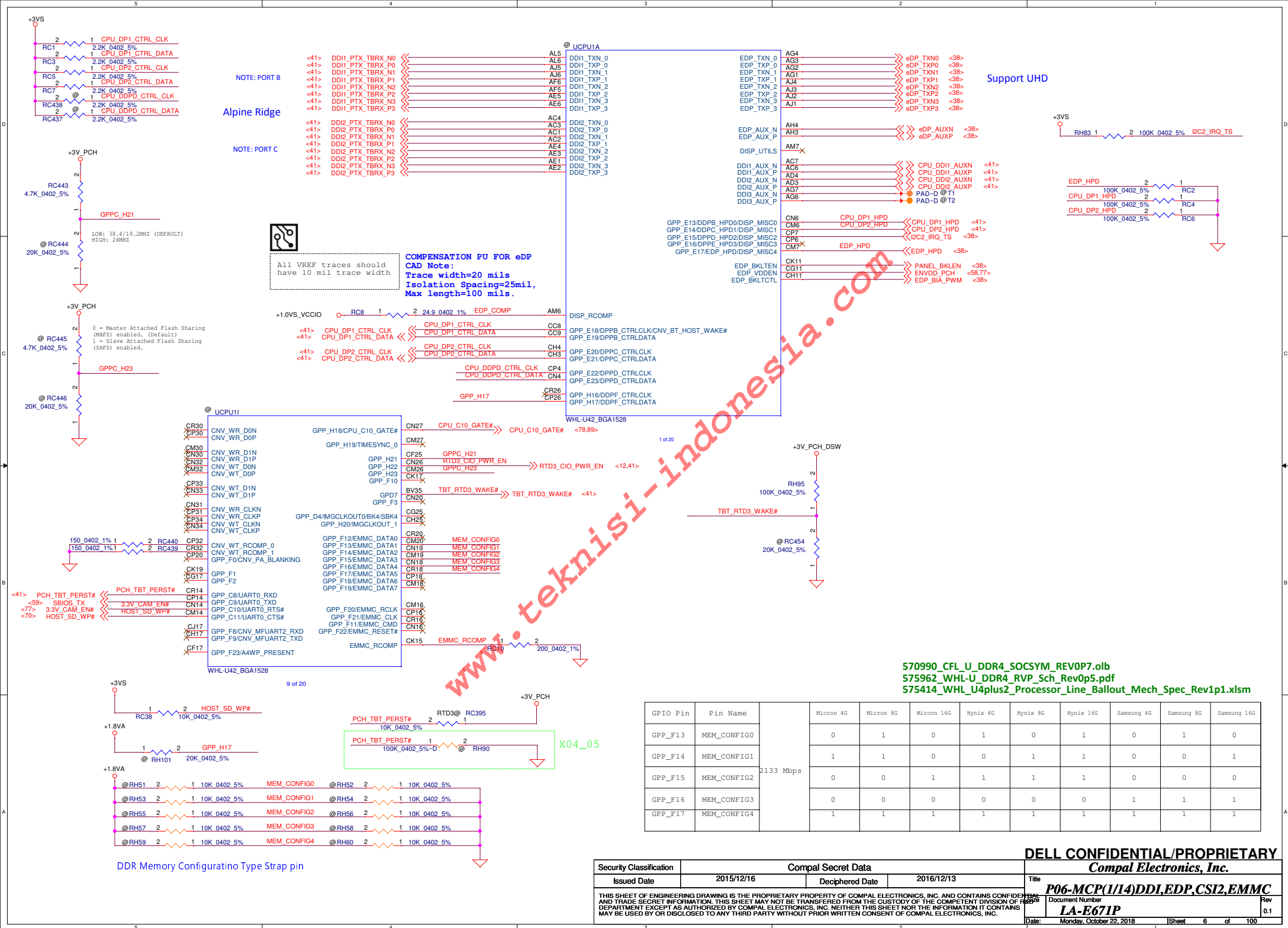
 : means Digital Ground
 : means Analog Ground



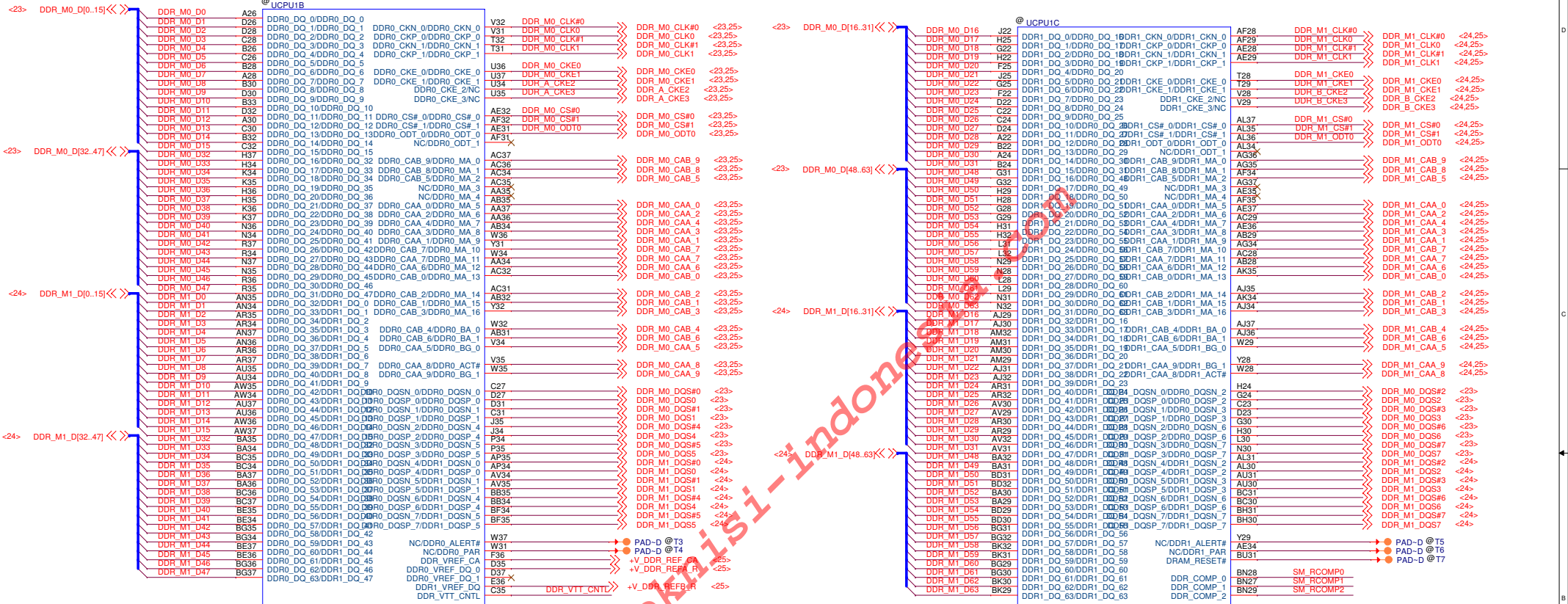
CPU PWR
PCH PWR
GPU PWR
Peripheral Device PWR

| | | | | | |
|-------------------------|--|--------------------|--|--------------------------------|--|
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| 2015/12/16 | | 2016/12/13 | | Title | |
| | | | | P04-Power rails | |
| | | | | Document Number | |
| | | | | LA-E671P | |
| | | | | Rev | |
| | | | | 0.1 | |
| | | | | Date: Monday, October 22, 2018 | |
| | | | | Sheet 4 of 100 | |

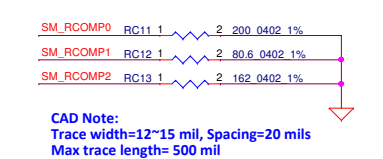




LPDDR3, Ballout for side by side(Non-Interleave)

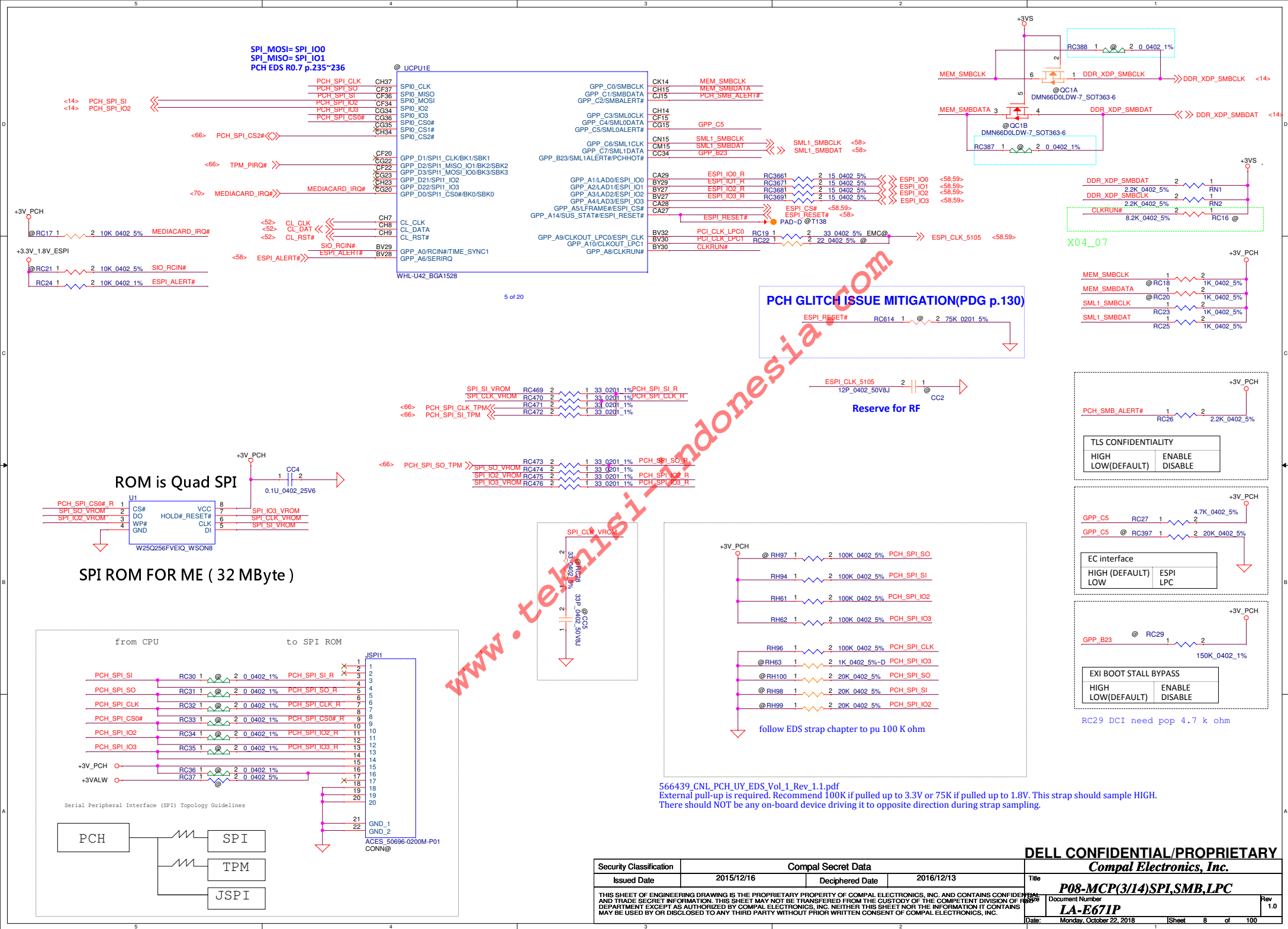


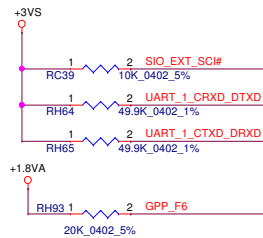
LPDDR3 COMPENSATION SIGNALS



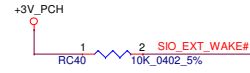
CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

| | | | | | |
|--|------------|--------------------|------------|---|--|
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| | | | | Document Number | |
| | | | | LA-E671P | |
| | | | | Rev 0.1 | |
| | | | | Date: Monday, October 22, 2018 | |
| | | | | Sheet 7 of 100 | |
| | | | | | |

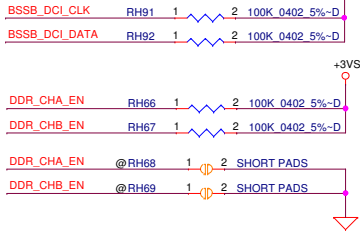
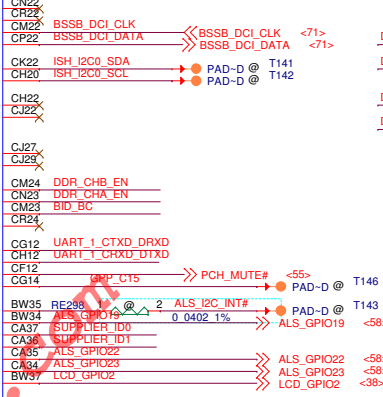
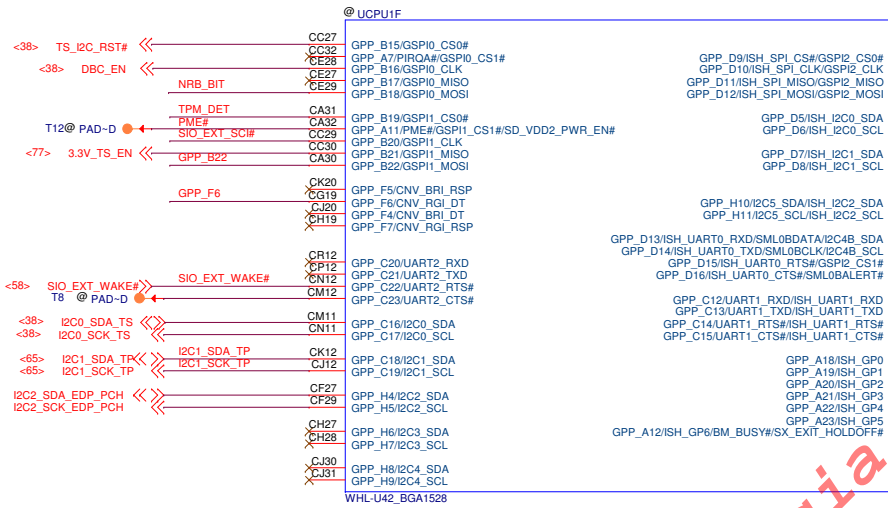




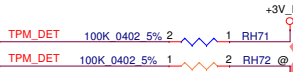
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.
(Disable CNVi for bring up)



TS
TP
eDP
PWRMONITOR

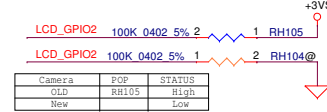


6 of 20

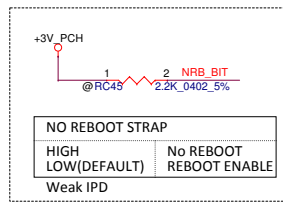


TPM BOM Optional

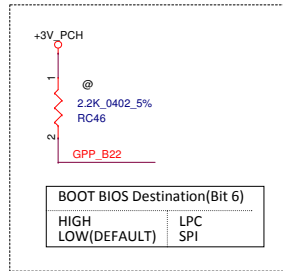
| TPM DET | |
|---------|--------------------------|
| TPM | 1 = W/TPM 0 = W/O TPM |



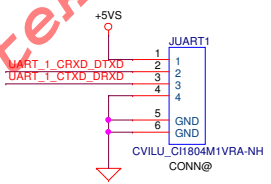
| Camera | POP | STATUS |
|--------|-------|--------|
| Old | RH105 | High |
| New | | Low |



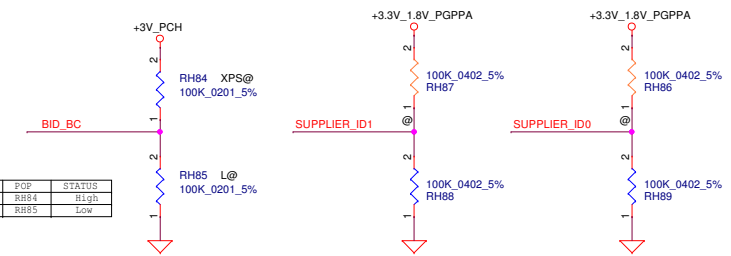
| NO REBOOT STRAP | |
|----------------------|----------------------------|
| HIGH LOW(DEFAULT) | No REBOOT REBOOT ENABLE |
| Weak IPD | |



| BOOT BIOS Destination(Bit 6) | |
|------------------------------|------------|
| HIGH LOW(DEFAULT) | LPC SPI |



| Product | POP | STATUS |
|---------|------|--------|
| XPS | RH84 | High |
| L | RH85 | Low |



| RH87 | RH88 | RH86 | RH89 | | REV |
|------|------|------|------|-----|------------|
| | V | | V | 0 0 | Supplier A |
| | V | V | | 0 1 | Supplier B |
| V | | | V | 1 0 | Supplier C |
| V | | V | | 1 1 | Supplier D |

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| | | | Rev LA-E671P |
| | | | Date: Monday, October 22, 2018 Sheet 9 of 100 |

Cardreader
PCIe Gen2 x 1

<70> PCIE_PRX_CARDTX_N5
<70> PCIE_PRX_CARDTX_P5
<70> PCIE_PTX_CARDRX_N5
<70> PCIE_PTX_CARDRX_P5

WLAN
PCIe Gen2 x 1

<52> PCIE_PRX_WLANTX_N7
<52> PCIE_PRX_WLANTX_P7
<52> PCIE_PTX_WLANRX_N7
<52> PCIE_PTX_WLANRX_P7

Alpine Ridge
PCIe Gen3 x 4

<41> PCIE_PRX_TBTX_N9
<41> PCIE_PRX_TBTX_P9
<41> PCIE_PTX_TBRX_N9
<41> PCIE_PTX_TBRX_P9

<41> PCIE_PRX_TBTX_N10
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<41> PCIE_PTX_TBRX_P10

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<41> PCIE_PTX_TBRX_P12

M.2 SSD
PCIe Gen3 x 4

<67> PCIE_PRX_SSDTX_N13
<67> PCIE_PRX_SSDTX_P13
<67> PCIE_PTX_SSDRX_N13
<67> PCIE_PTX_SSDRX_P13

<67> PCIE_PRX_SSDTX_N14
<67> PCIE_PRX_SSDTX_P14
<67> PCIE_PTX_SSDRX_N14
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<67> PCIE_PRX_SSDTX_P15
<67> PCIE_PTX_SSDRX_N15
<67> PCIE_PTX_SSDRX_P15

<67> SATA_CRX_DTX_N2
<67> SATA_CRX_DTX_P2
<67> SATA_CTX_DRX_N2
<67> SATA_CTX_DRX_P2

SATA SSD

<67> PCIE_RCOMP_N
<67> PCIE_RCOMP_P

<67> GPP_H12M2_SKT2/CFG_0
<67> GPP_H13M2_SKT3/CFG_1
<67> GPP_H14M2_SKT2/CFG_2
<67> GPP_H15M2_SKT2/CFG_3

@UCPU1H

PCIE5_RXN/USB31_5_RXN
PCIE5_RXP/USB31_5_RXP
PCIE5_TXN/USB31_5_TXN
PCIE5_TXP/USB31_5_TXP

PCIE6_RXN/USB31_6_RXN
PCIE6_RXP/USB31_6_RXP
PCIE6_TXN/USB31_6_TXN
PCIE6_TXP/USB31_6_TXP

PCIE7_RXN
PCIE7_RXP
PCIE7_TXN
PCIE7_TXP

PCIE8_RXN
PCIE8_RXP
PCIE8_TXN
PCIE8_TXP

PCIE9_RXN
PCIE9_RXP
PCIE9_TXN
PCIE9_TXP

PCIE10_RXN
PCIE10_RXP
PCIE10_TXN
PCIE10_TXP

PCIE11_RXN/SATA0_RXN
PCIE11_RXP/SATA0_RXP
PCIE11_TXN/SATA0_TXN
PCIE11_TXP/SATA0_TXP

PCIE12_RXN/SATA1A_RXN
PCIE12_RXP/SATA1A_RXP
PCIE12_TXN/SATA1A_TXN
PCIE12_TXP/SATA1A_TXP

PCIE13_RXN
PCIE13_RXP
PCIE13_TXN
PCIE13_TXP

PCIE14_RXN
PCIE14_RXP
PCIE14_TXN
PCIE14_TXP

PCIE15_RXN/SATA1B_RXN
PCIE15_RXP/SATA1B_RXP
PCIE15_TXN/SATA1B_TXN
PCIE15_TXP/SATA1B_TXP

PCIE16_RXN/SATA2_RXN
PCIE16_RXP/SATA2_RXP
PCIE16_TXN/SATA2_TXN
PCIE16_TXP/SATA2_TXP

PCIE_RCOMP_N
PCIE_RCOMP_P

GPP_H12M2_SKT2/CFG_0
GPP_H13M2_SKT3/CFG_1
GPP_H14M2_SKT2/CFG_2
GPP_H15M2_SKT2/CFG_3

UFS_RESET#

8 of 20

PCIE1_RXN/USB31_1_RXN
PCIE1_RXP/USB31_1_RXP
PCIE1_TXN/USB31_1_TXN
PCIE1_TXP/USB31_1_TXP

PCIE2_RXN/USB31_2_RXN/SSIC_1_RXN
PCIE2_RXP/USB31_2_RXP/SSIC_1_RXP
PCIE2_TXN/USB31_2_TXN/SSIC_1_TXN
PCIE2_TXP/USB31_2_TXP/SSIC_1_TXP

PCIE3_RXN/USB31_3_RXN
PCIE3_RXP/USB31_3_RXP
PCIE3_TXN/USB31_3_TXN
PCIE3_TXP/USB31_3_TXP

PCIE4_RXN/USB31_4_RXN
PCIE4_RXP/USB31_4_RXP
PCIE4_TXN/USB31_4_TXN
PCIE4_TXP/USB31_4_TXP

USB2_1N
USB2_1P
USB2_2N
USB2_2P

USB2_3N
USB2_3P
USB2_4N
USB2_4P

USB2_5N
USB2_5P
USB2_6N
USB2_6P

USB2_7N
USB2_7P
USB2_8N
USB2_8P

USB2_9N
USB2_9P
USB2_10N
USB2_10P

USB2_COMP
USB2_ID
USB2_VBUSSENSE

GPP_E9/USB2_OC0#/GP_BSSB_CLK
GPP_E10/USB2_OC1#/GP_BSSB_DI
GPP_E11/USB2_OC2#
GPP_E12/USB2_OC3#

GPP_E4/DEVSLP0
GPP_E5/DEVSLP1
GPP_E6/DEVSLP2

GPP_E0/SATA0PCIE0/SATAGP0
GPP_E1/SATA0PCIE1/SATAGP1
GPP_E2/SATA0PCIE2/SATAGP2

GPP_E8/SATALED#/SPI1_CS1#
UFS_RESET#

USB3_CRX_DTX_N1
USB3_CRX_DTX_P1
USB3_CTX_DRX_N1
USB3_CTX_DRX_P1

USB3R4
USB3TN4
USB3TP4

USB20_N1
USB20_P1

USB20_N5
USB20_P5

USB20_N6
USB20_P6
USB20_N7
USB20_P7

USB20_N8
USB20_P8

USB20_N9
USB20_P9
USB20_N10
USB20_P10

TBT_A_USB_OC0#
TBT_B_USB_OC1#
MUX_C_USB_OC2#
MUX_C_USB_OC3#

B+ CAM_EN
PRIM_CORE_OPT_DIS
SSD_DEVSLP

SSD_IFDET

USB3.0 DP MX (PS8802)

DCI Debug

USB2.0 for USB PD PORT3

CAM & IR CAM

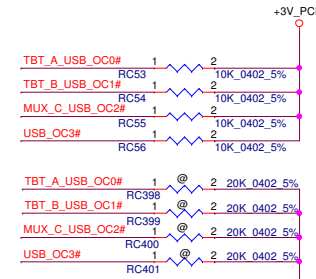
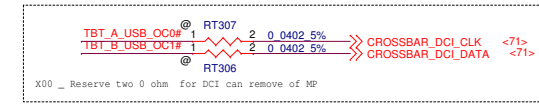
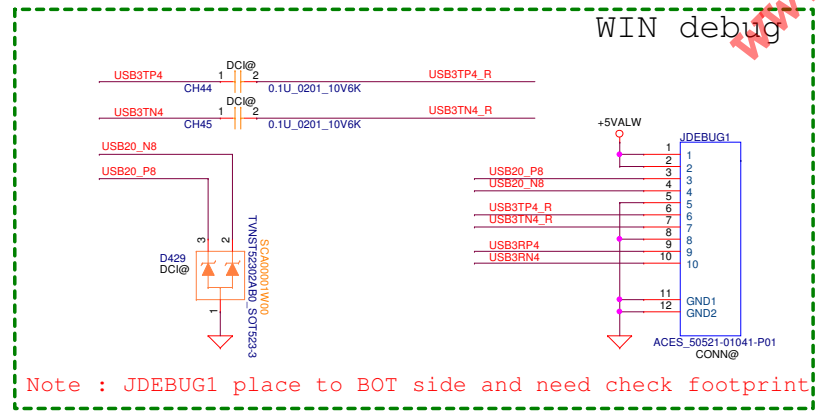
USB2.0 for USB PD PORT2

NGFF (WLAN)

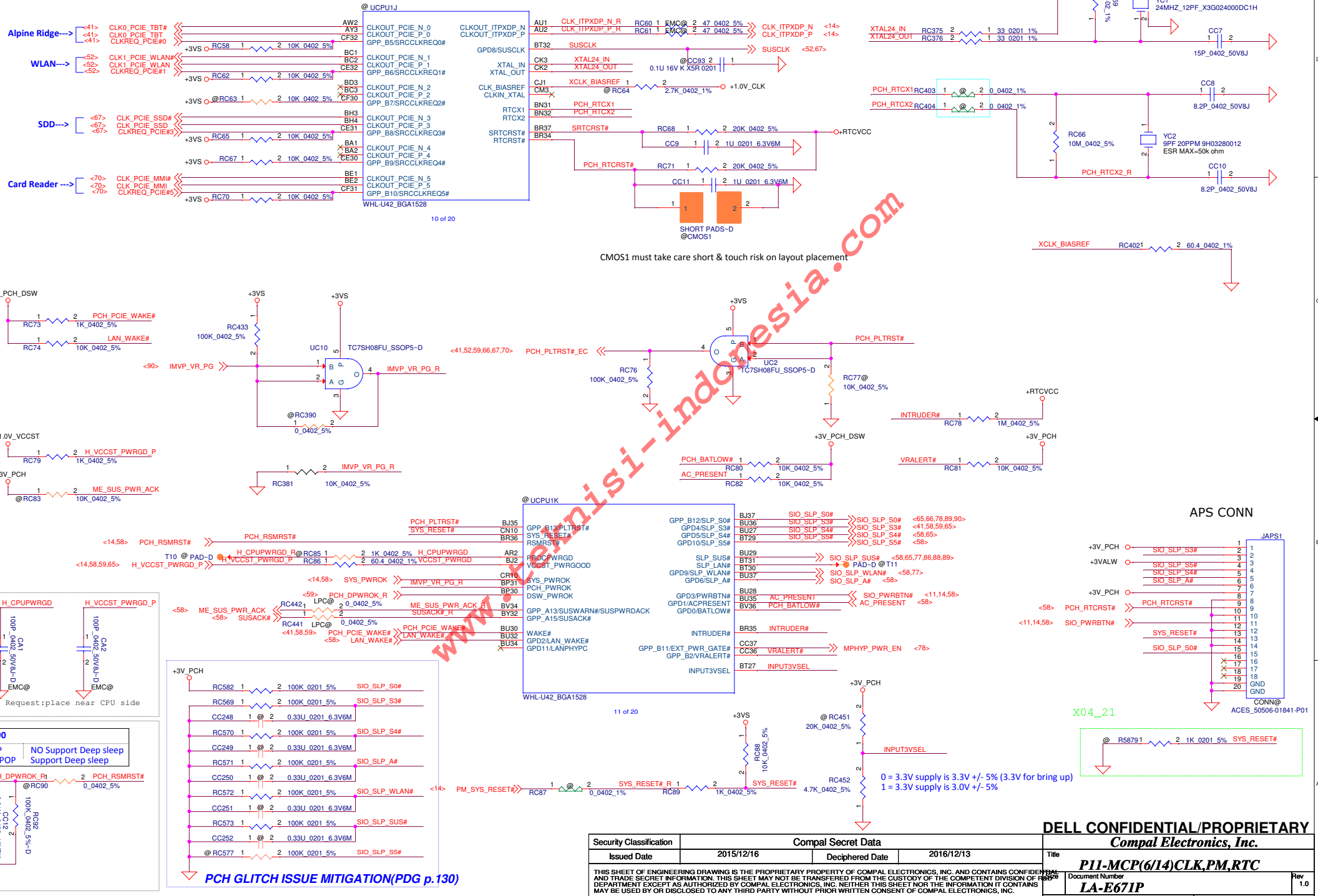
USB2.0 for DCI

USB2.0 for USB PD PORT1

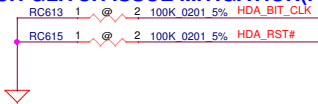
Fingerprint



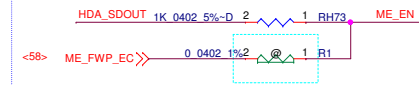
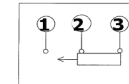
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| | | 2016/12/13 | | Title | |
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| | | | | Document Number | |
| | | | | LA-E671P | |
| | | | | Date: Monday, October 22, 2018 | |
| | | | | Sheet 10 of 100 | |
| | | | | Rev 1.0 | |
| | | | | | |



PCH GLITCH ISSUE MITIGATION(PDG p.130)



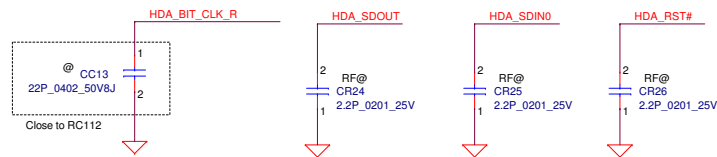
Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.



ME_FWP PCH has internal 20K PD.

FLASH DESCRIPTOR SECURITY OVERRIDE

Disable ME Protect (ME can be updated) ----> Pin1 & Pin2 short
Enable ME Protect (ME cannot be updated)-->Pin3 & Pin2 short(Default position)



<55> HDA_SYNC_R
<55> HDA_BIT_CLK_R
<55> HDA_SDOOUT_R
<55> HDA_SDIIN0

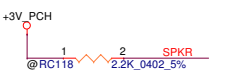
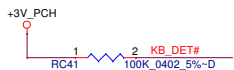
RC111 1 2 33 0402 5% HDA_SYNC
RC112 1 2 33 0402 5% HDA_BIT_CLK
RC113 1 2 33 0402 5% HDA_SDOOUT
HDA_SDIIN0

<41> RTD3_USB_PWR_EN

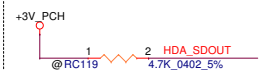
PAD-D @ T15 HDA_RST#

<6,41> RTD3_CIO_PWR_EN
<41> TBT_FORCE_PWR
<41> TBT_BATLOW#
<64> KB_DET#

RC462 1 2 0 0402 5%
RC461 1 2 0 0402 1%
RC457 1 2 0 0402 1%
RC463 1 2 0 0402 1%



TOP SWAP STRAP
HIGH LOW(DEFAULT) ENABLE DISABLE



Flash Descriptor Security override
HIGH LOW(DEFAULT) DISABLE ENABLE

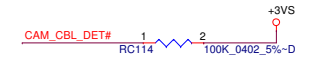


7 of 20

GPP_G0/SD_CMD
GPP_G1/SD3_DATA0
GPP_G2/SD3_DATA1
GPP_G3/SD3_DATA2
GPP_G4/SD3_DATA3
GPP_G5/SD_CD#
GPP_G6/SD_CLK
GPP_G7/SD_WP

ISH_GP7
PAD-D @ T144

SD_1P8_RCOMP
SD_3P0_RCOMP



CAM_CBL_DET# 1 2 100K_0402_5%-D

<38> CAM_CBL_DET#

<41> TBT_CIO_PLUG_EVENT#

<77> SSD_PWR_EN

<56> SPK_DET#

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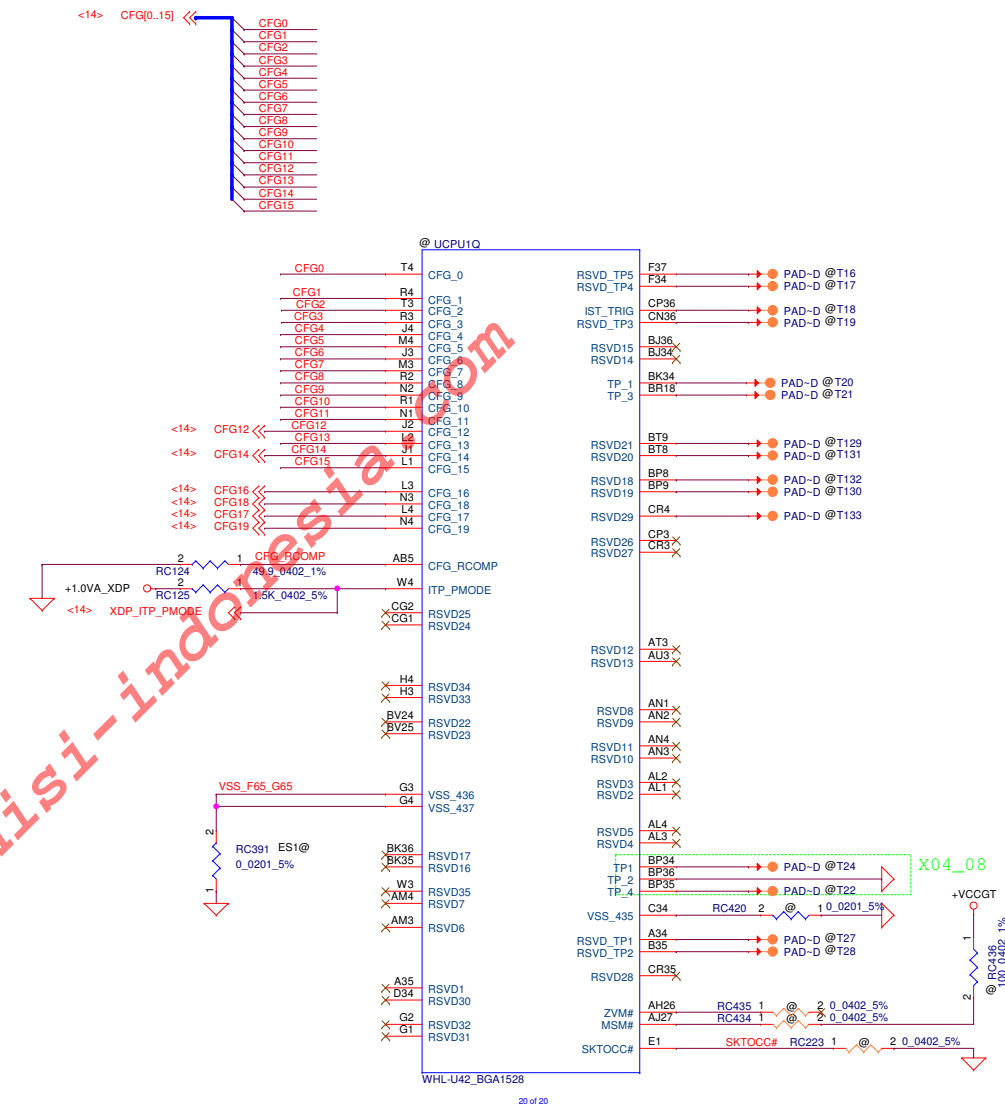
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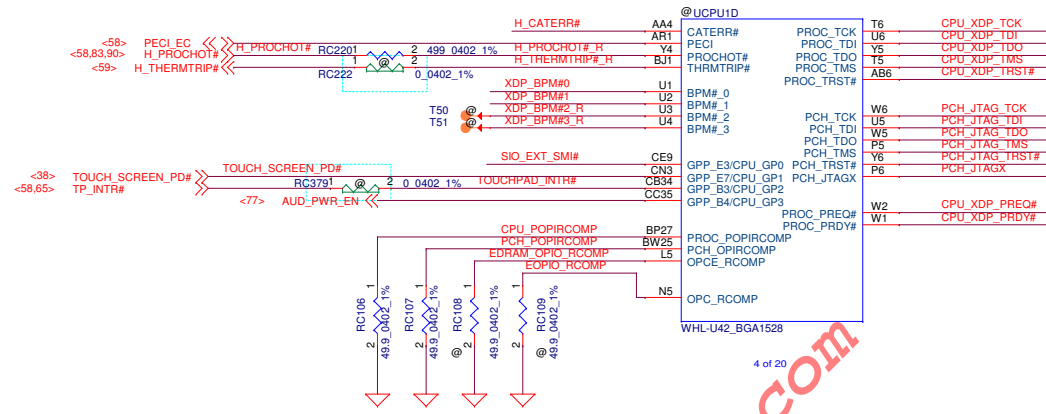
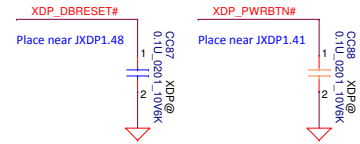
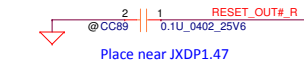
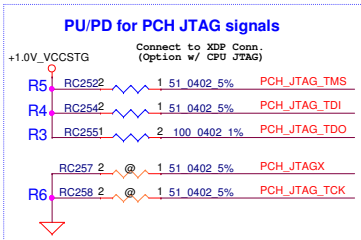
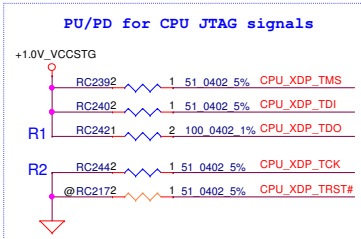
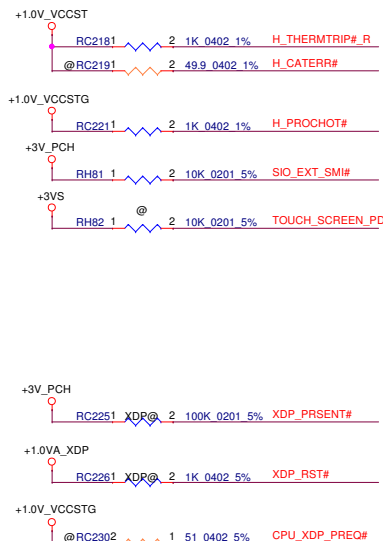
Title P12-MCP(7/14)MISC,ITAG,HDA,SDIO

Document Number LA-E671P

Date: Monday, October 22, 2018 Sheet 12 of 100

Rev 1.0



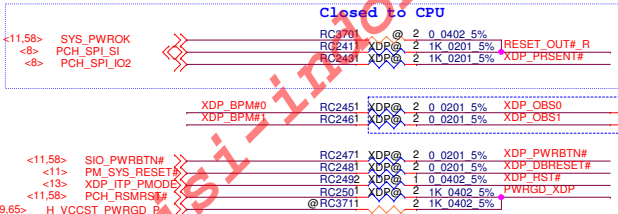


<To CPU JTAG>

| | | | | | | | |
|---------------|--------|------|---|---|------|----|-----------|
| CPU_XDP_TDO | RC2271 | XDP@ | 2 | 0 | 0201 | 5% | XDP_TDO |
| CPU_XDP_TCK | RC2281 | XDP@ | 2 | 0 | 0201 | 5% | XDP_TCK |
| CPU_XDP_TDI | RC2291 | XDP@ | 2 | 0 | 0201 | 5% | XDP_TDI |
| CPU_XDP_TMS | RC2311 | XDP@ | 2 | 0 | 0201 | 5% | XDP_TMS |
| CPU_XDP_TRST# | RC2321 | XDP@ | 2 | 0 | 0201 | 5% | XDP_TRST# |

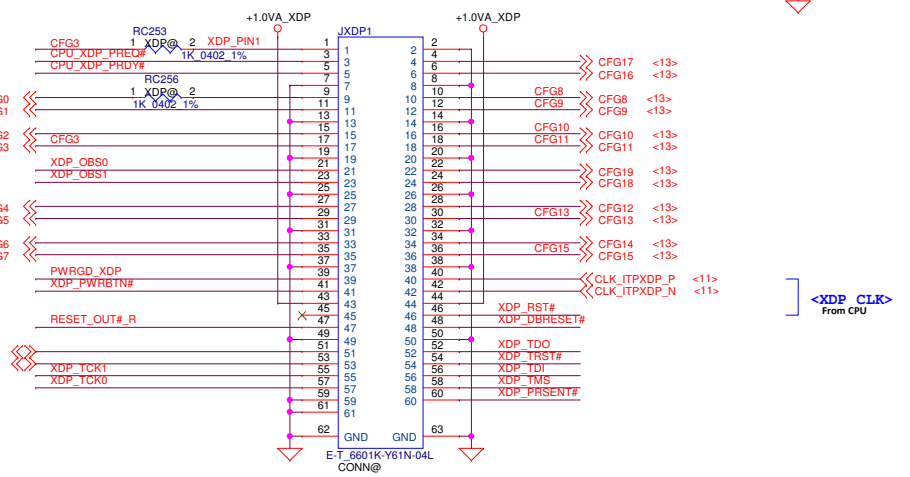
<To PCH JTAG>

| | | | | | | | |
|----------------|--------|------|---|---|------|----|-----------|
| PCH_JTAG_TDO | RC2331 | XDP@ | 2 | 0 | 0201 | 5% | XDP_TDO |
| PCH_JTAG_TDI | RC2341 | XDP@ | 2 | 0 | 0201 | 5% | XDP_TDI |
| PCH_JTAG_TMS | RC2351 | XDP@ | 2 | 0 | 0201 | 5% | XDP_TMS |
| PCH_JTAG_TRST# | RC2361 | XDP@ | 2 | 0 | 0201 | 5% | XDP_TRST# |
| PCH_JTAGX | RC2371 | XDP@ | 2 | 0 | 0201 | 5% | XDP_TCK0 |
| PCH_JTAG_TCK | RC2381 | XDP@ | 2 | 0 | 0201 | 5% | XDP_TCK1 |



<XDP Misc.>

XDP CONN

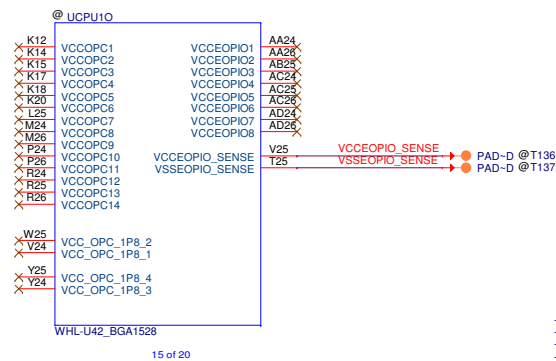


PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source

+VCC_CORE: 0.55~1.5V, 29A
+VCC_EDRAM: 1V, 2.5A

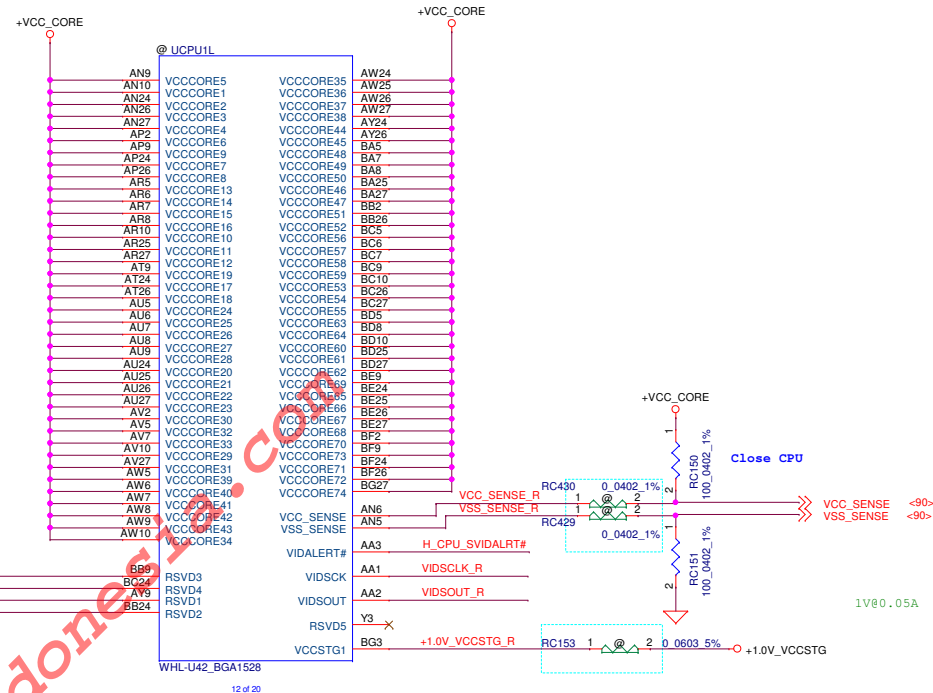
| Pin Number | CFL U42 | WHL U42 Q5/Production | CNL U22/WHL U42 E50/1 |
|------------|---------------|-----------------------|-----------------------|
| AH26 | ZV# | RSVD | RSVD |
| T25 | VSSGPIO_SENSE | RSVD | RSVD |
| V25 | VCCGPIO_SENSE | RSVD | RSVD |
| AA24 | VCCGPIO | RSVD | RSVD |
| AA26 | VCCGPIO | RSVD | RSVD |
| AB25 | VCCGPIO | RSVD | RSVD |
| AC24 | VCCGPIO | RSVD | RSVD |
| AC25 | VCCGPIO | RSVD | RSVD |
| AC26 | VCCGPIO | RSVD | RSVD |
| AD24 | VCCGPIO | RSVD | RSVD |
| AD26 | VCCGPIO | RSVD | RSVD |
| K12 | VCCOPC | RSVD | RSVD |
| K14 | VCCOPC | RSVD | RSVD |
| K15 | VCCOPC | RSVD | RSVD |
| K17 | VCCOPC | RSVD | RSVD |
| K18 | VCCOPC | RSVD | RSVD |
| K20 | VCCOPC | RSVD | RSVD |
| L25 | VCCOPC | RSVD | RSVD |
| M24 | VCCOPC | RSVD | RSVD |
| M26 | VCCOPC | RSVD | RSVD |
| P24 | VCCOPC | RSVD | RSVD |
| P26 | VCCOPC | RSVD | RSVD |
| R24 | VCCOPC | RSVD | RSVD |
| R25 | VCCOPC | RSVD | RSVD |
| R26 | VCCOPC | RSVD | RSVD |
| W25 | VCC_OPC_1P8_2 | RSVD | RSVD |
| V24 | VCC_OPC_1P8_1 | RSVD | RSVD |
| Y25 | VCC_OPC_1P8_4 | RSVD | RSVD |
| Y24 | VCC_OPC_1P8_3 | RSVD | RSVD |
| K18 | VCCOPC | RSVD | RSVD |
| K20 | VCCOPC | RSVD | RSVD |
| L25 | VCCOPC | RSVD | RSVD |
| M24 | VCCOPC | RSVD | RSVD |
| M26 | VCCOPC | RSVD | RSVD |
| P24 | VCCOPC | RSVD | RSVD |
| P26 | VCCOPC | RSVD | RSVD |
| R24 | VCCOPC | RSVD | RSVD |
| R25 | VCCOPC | RSVD | RSVD |
| R26 | VCCOPC | RSVD | RSVD |
| Y24 | VCC_OPC_1P8 | RSVD | RSVD |
| Y25 | VCC_OPC_1P8 | RSVD | RSVD |
| W25 | VCC_OPC_1P8 | RSVD | RSVD |
| AI27 | MSM# | RSVD | RSVD |
| G4 | VSS | RSVD | RSVD |
| G3 | VSS | RSVD | RSVD |
| G4 | VSS | RSVD | RSVD |



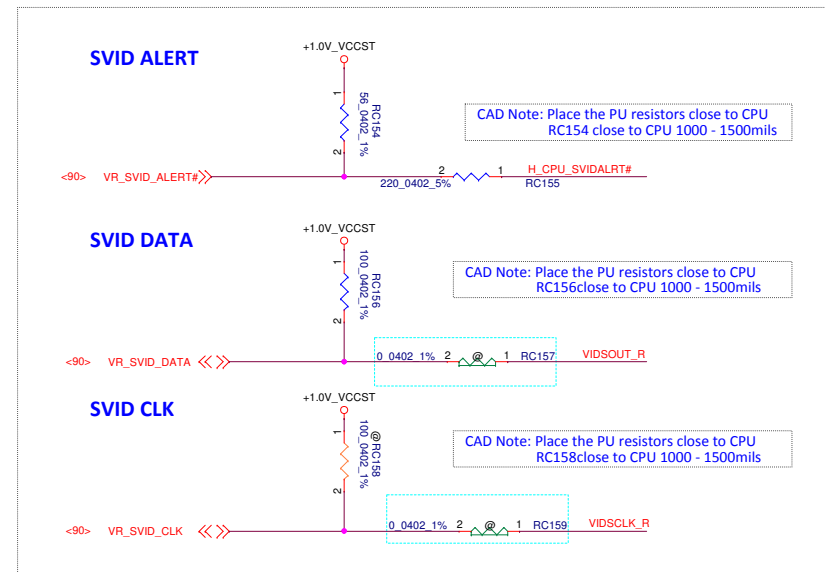
+V1.8S_EDRAM: 1.8V, 50mA - REMOVE
+VCC_EGPIO: 0.8~1V, 2A - REMOVE

T29 @ PAD-D
T30 @ PAD-D
T134 @ PAD-D
T135 @ PAD-D

+VCC_CORE G0
+VCC_CORE G1
+VCC_CORE G2
+VCC_CORE G3



VCCOPC,VCCOPC_1P8,VCCGPIO for SKYLAKE-U 2+3e
(w/ on package cache)



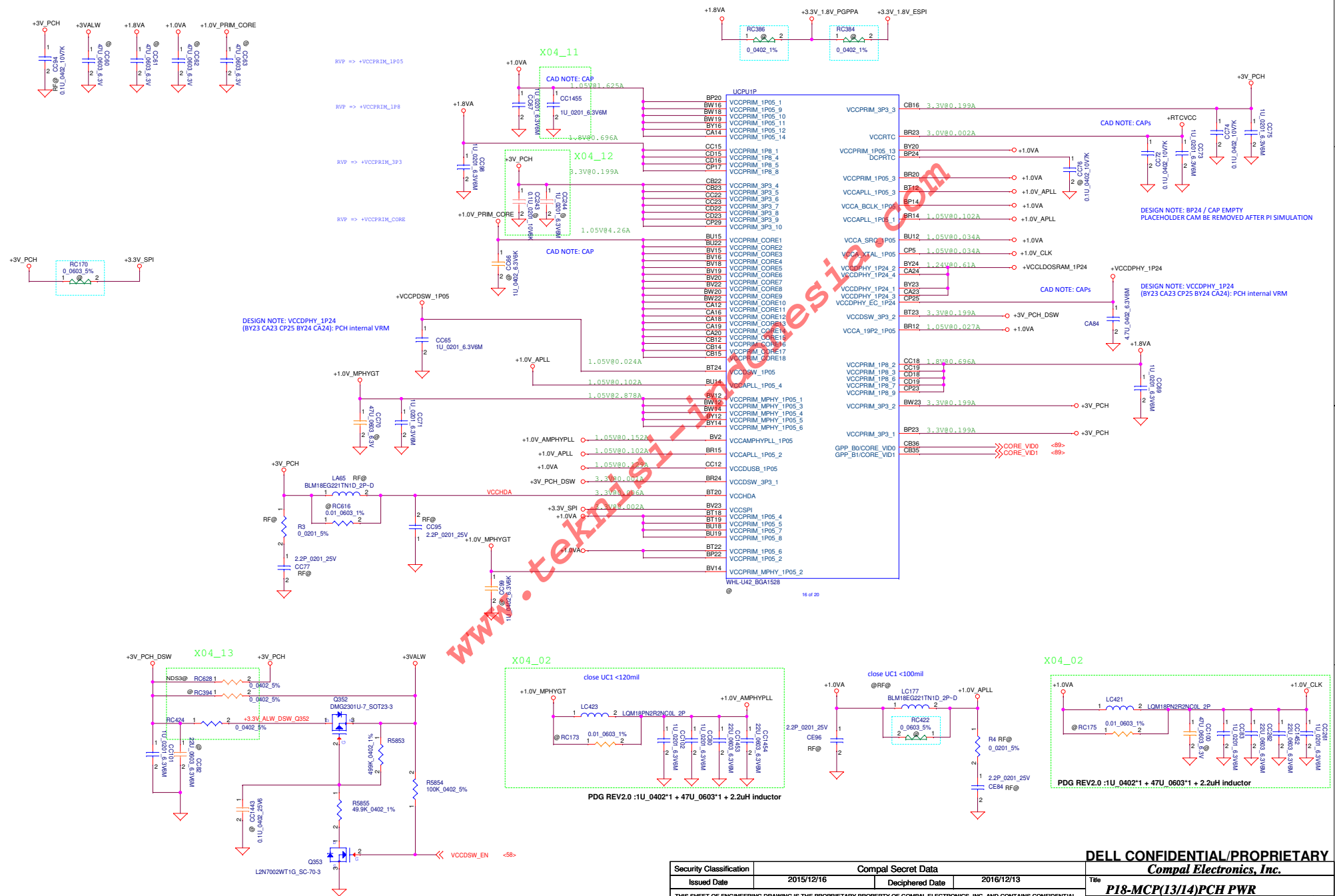
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|-----------------|----------------------------|-----------------|
| Title | P15-MCP(10/14)PWR-VCC CORE | |
| Document Number | LA-E671P | |
| Date | Monday, October 22, 2018 | Sheet 15 of 100 |

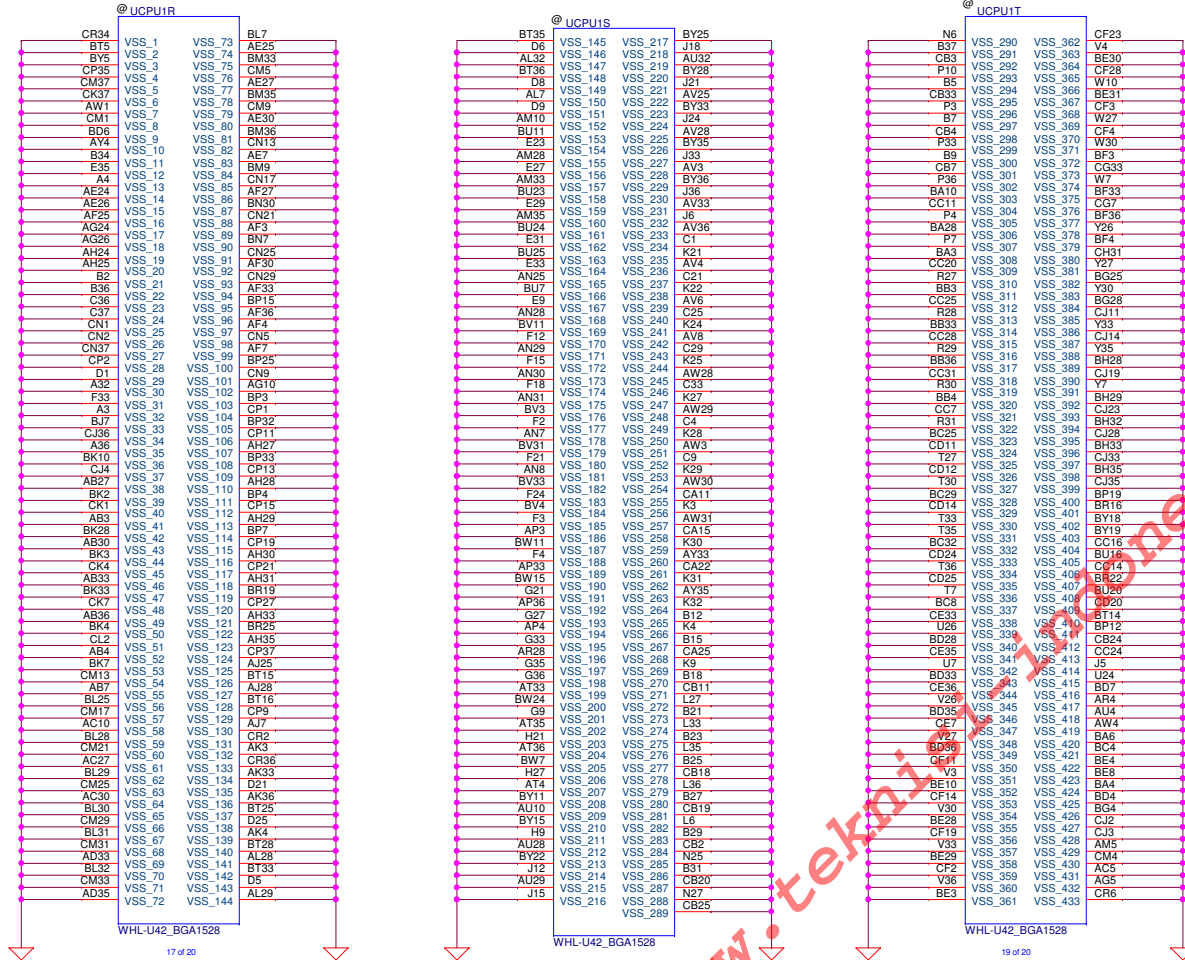
PCH PWR



| | |
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Note1: VCCPRIM_CORE Implementation with PCH CORE_VID Recommendation



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| | | | | Sheet 20 of 100 | | |

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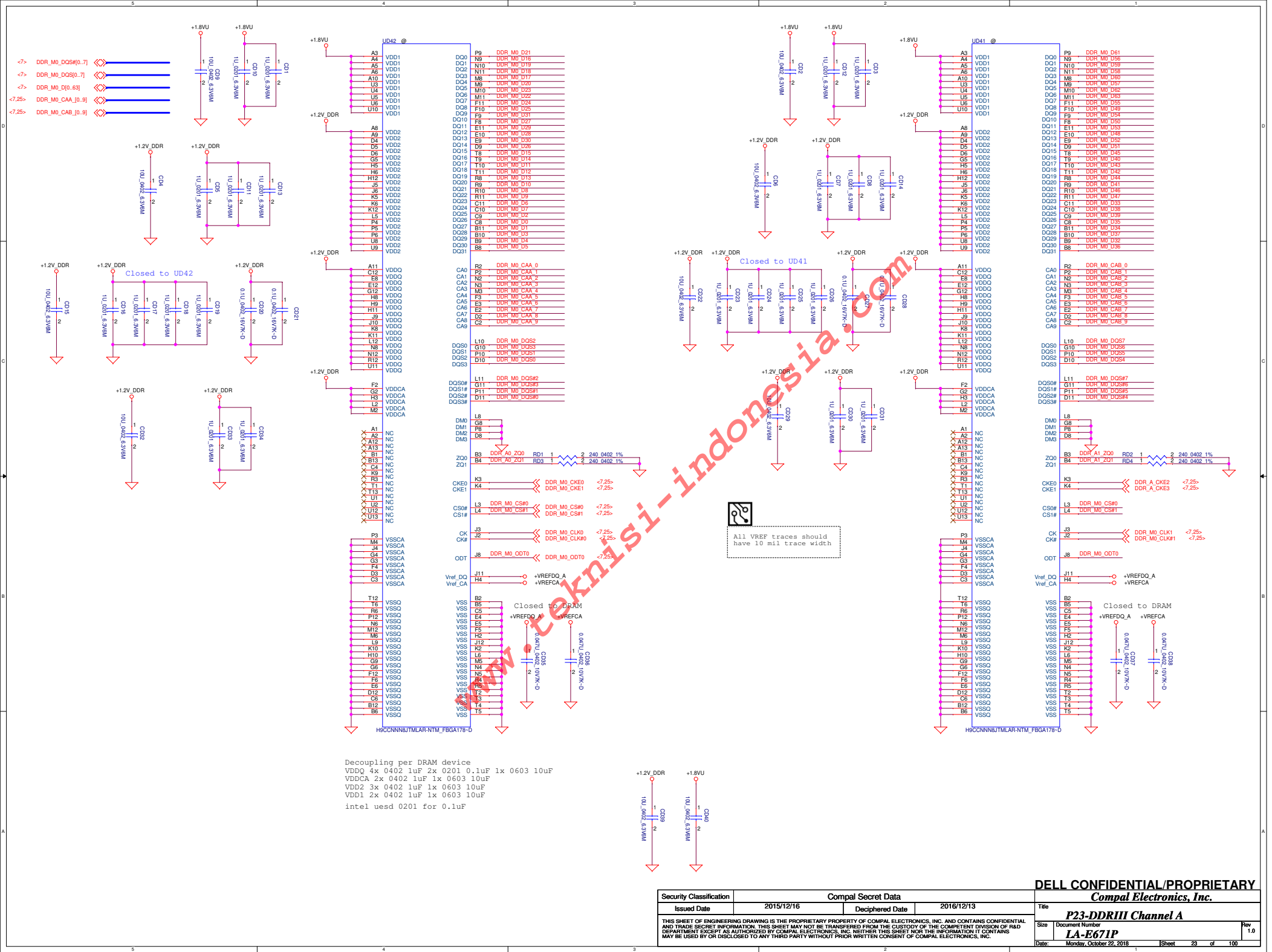
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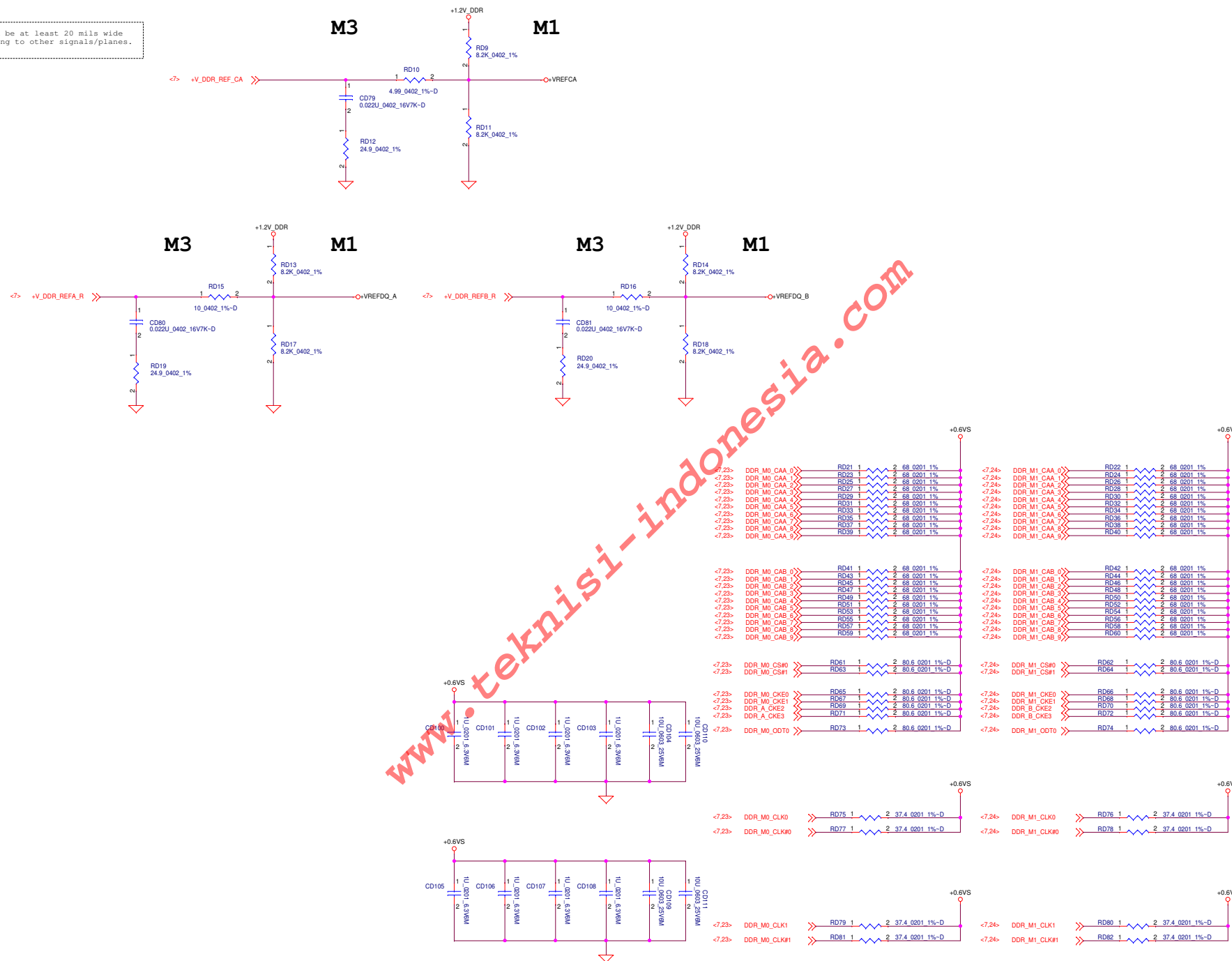
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VREF traces should be at least 20 mils wide
with 20 mils spacing to other signals/planes.



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| | | | | Document Number | |
| | | | | LA-E671P | |
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| | | | | Sheet | |
| | | | | 25 of 100 | |
| | | | | Rev | |
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| | | | | P035 - Reserve | |
| | | | | Size | Rev |
| | | | | Document Number | 0.1 |
| | | | | LA-E671P | |
| | | | | Date: | Monday, October 22, 2018 |
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| | | | | P036 - Reserve | |
| | | | | Size | Rev |
| | | | | Document Number | 0.1 |
| | | | | LA-E671P | |
| | | | | Date: | Monday, October 22, 2018 |
| | | | | Sheet | 36 of 100 |

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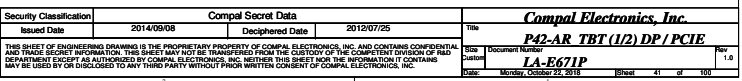
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| Security Classification | | Compal Secret Data | | DELL CONFIDENTIAL/PROPRIETARY | |
| Issued Date | | 2018/01/23 | Deciphered Date | Compal Electronics, Inc. | |
| | | | 2022/12/31 | Title | |
| | | | | P037 - Reserve | |
| | | | | Size | Rev |
| | | | | Document Number | 0.1 |
| | | | | LA-G441P | |
| | | | | Date: | Monday, October 22, 2018 |
| | | | | Sheet | 37 of 100 |

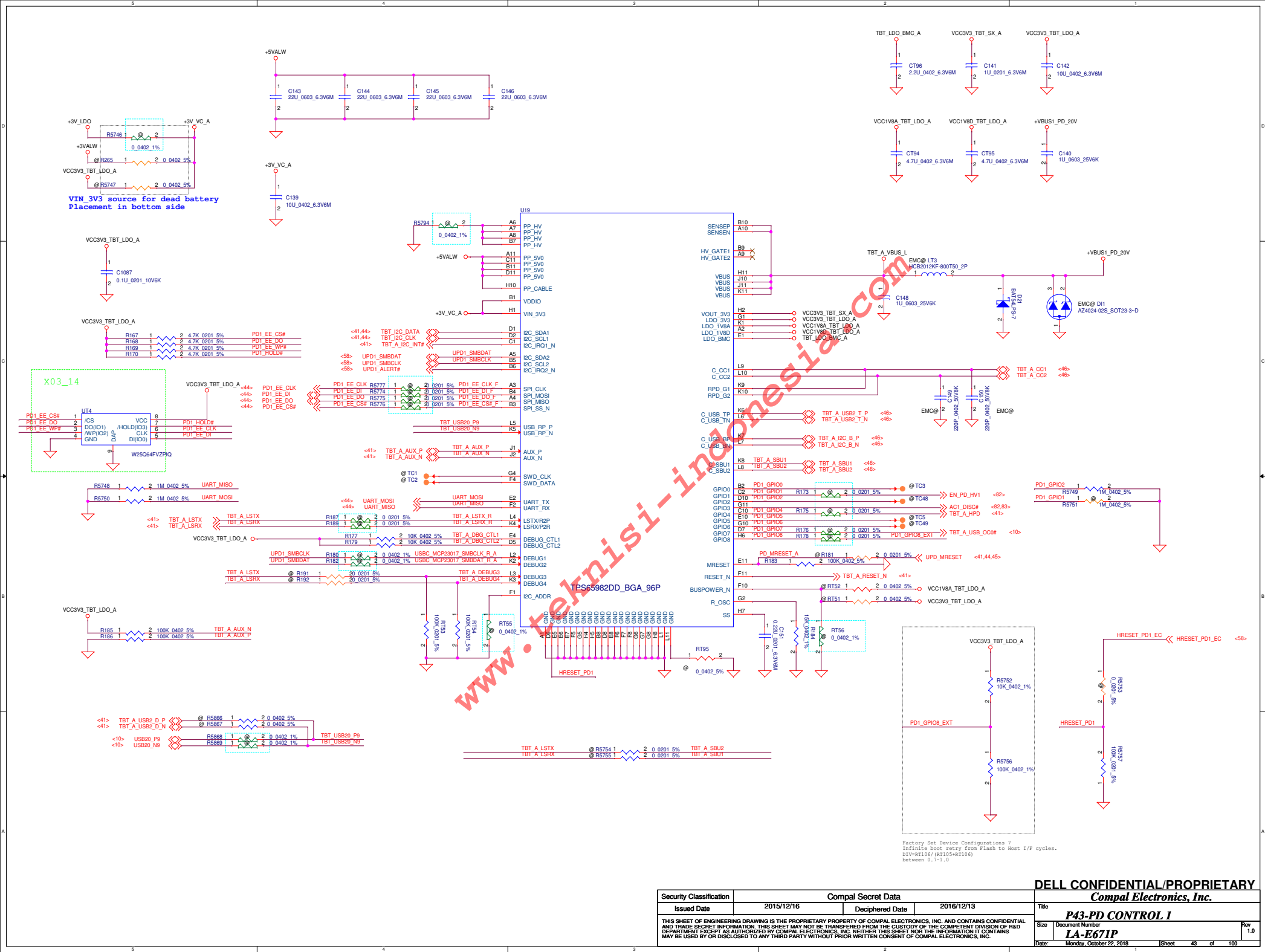
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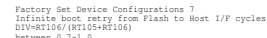
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| Security Classification | | Compal Secret Data | | DELL CONFIDENTIAL/PROPRIETARY | |
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| | | | | Document Number | |
| | | | | LA-E671P | |
| | | | | Rev | |
| | | | | 0.1 | |
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| | | | | Sheet 40 of 100 | |



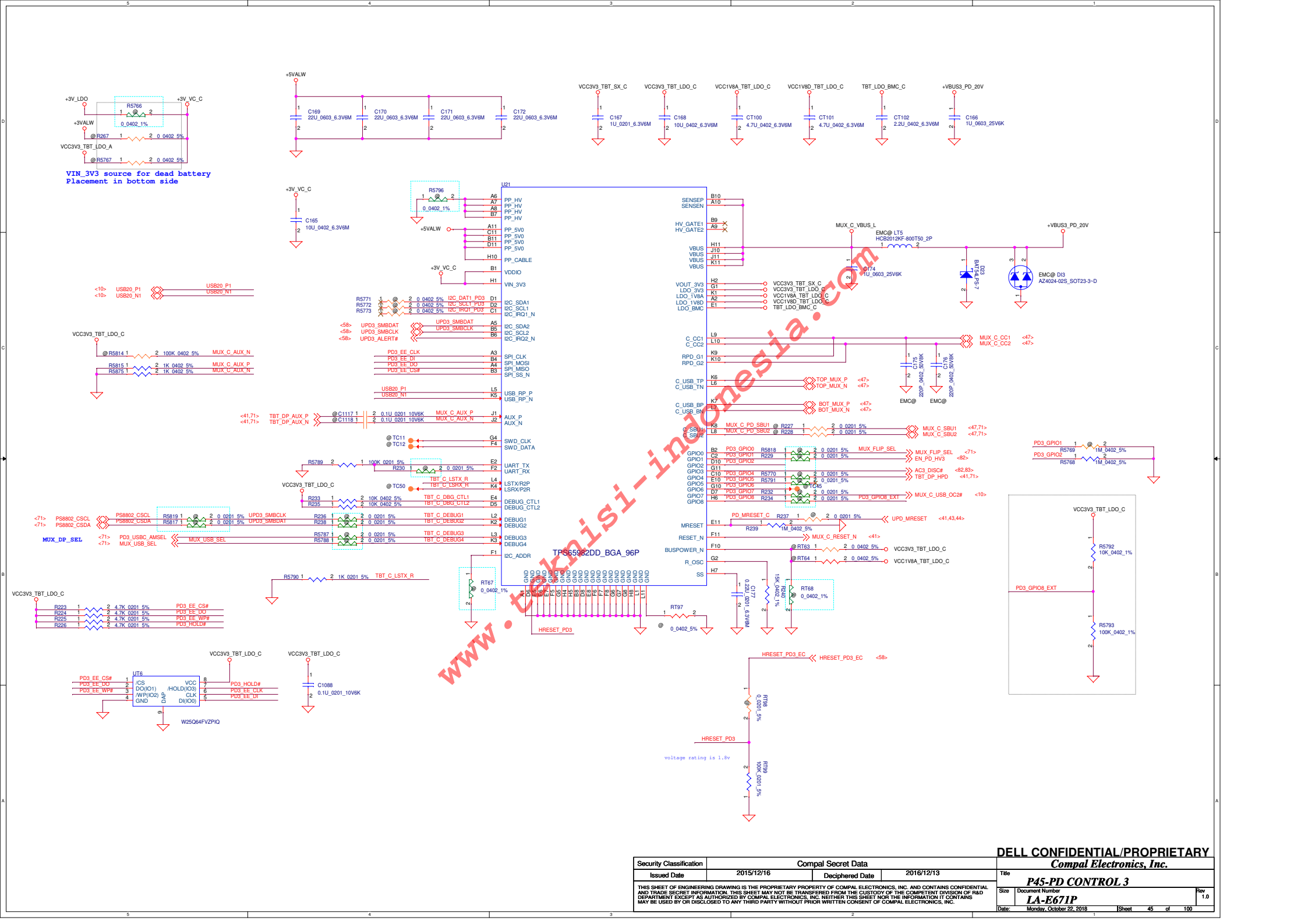


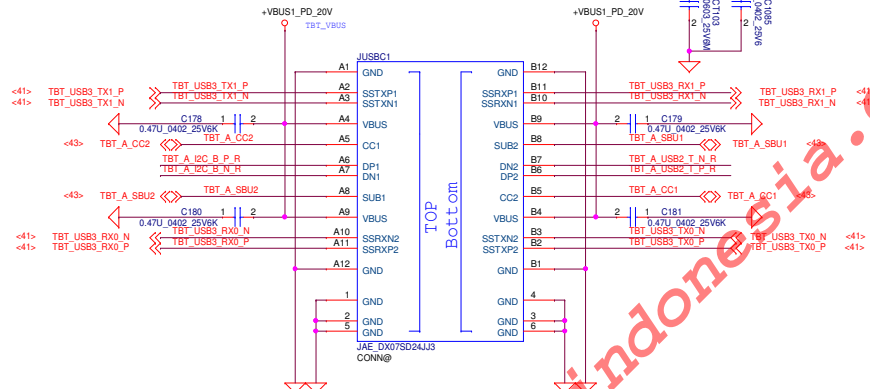
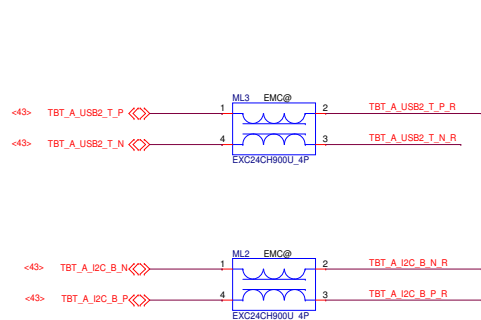
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| Security Classification | Compal Secret Data | | | <div style="text-align: center;"> CONFIDENTIAL PROPRIETARY Compal Electronics, Inc. </div> | | |
| Issued Date | 2015/12/16 | Deciphered Date | 2016/12/13 | <div style="text-align: center;"> P43-PD CONTROL 1 LA-E671P </div> | | |
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| | | | | Date: Monday, October 22, 2018 Sheet 43 of 100 | | |



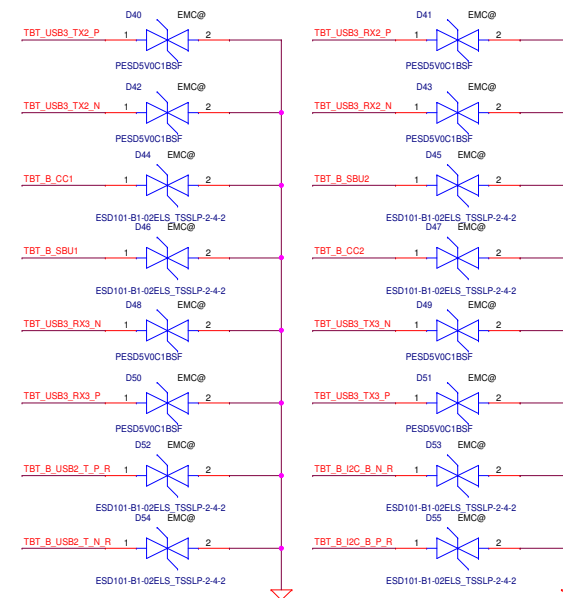
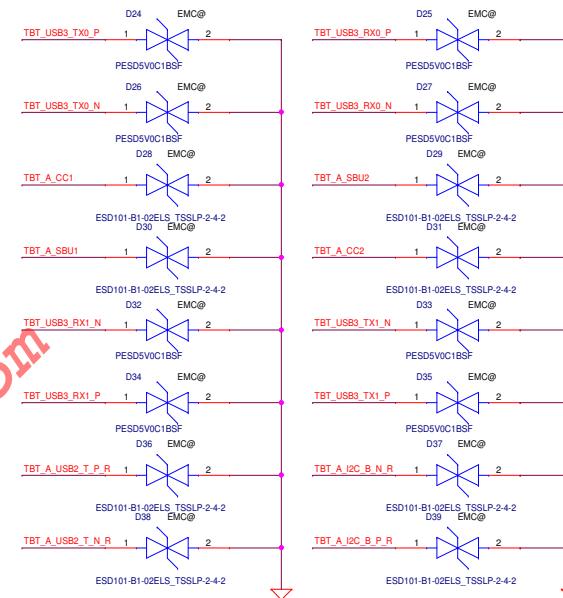
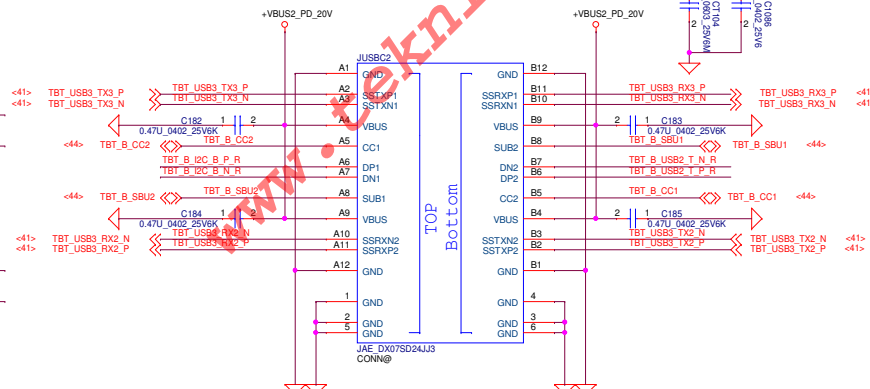
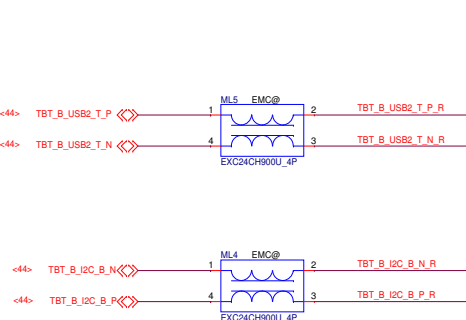
Date: Monday, October 22, 2018 Sheet 44 of 100

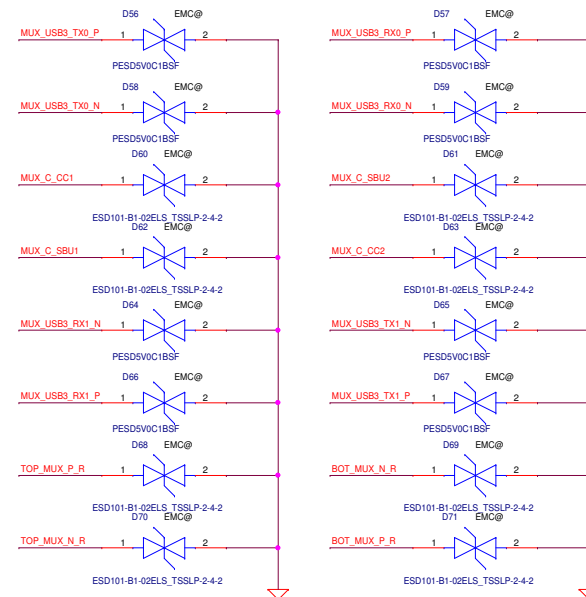
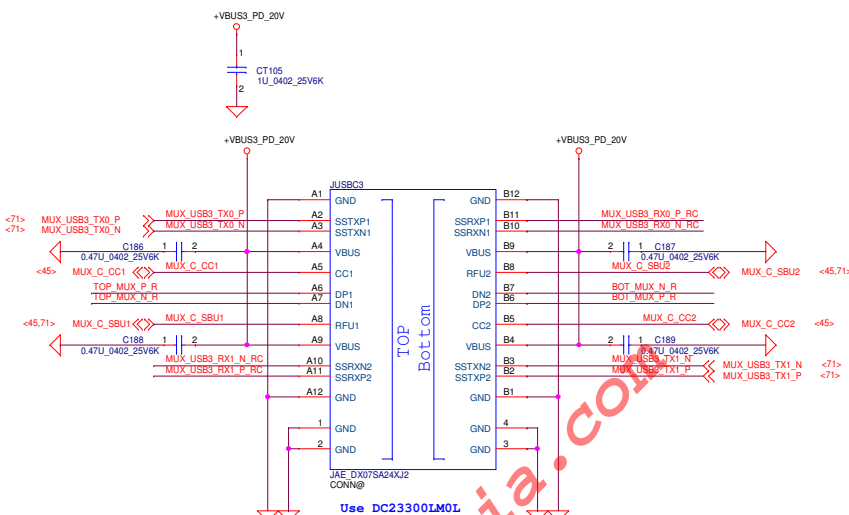
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| Security Classification | | Compal Secret Data | | <div>DECLASSIFIED/CONFIDENTIAL</div> <div>Compal Electronics, Inc.</div> | |
| Issued Date | 2015/12/16 | Deciphered Date | 2016/12/13 | <div>Title</div> <div>P44-PD CONTROL 2</div> | |
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| | | | | Document Number | 1.0 |
| | | | | LA-E671P | |
| | | | | Date: Monday, October 22, 2018 | Sheet 44 of 100 |





JUSBC1 and JUSBC2 use SP060009R01





Notes

Crp Cap Value: 297nF to 363nF including tolerance

Recommended Short Protection

USB3pl_Type_C_ECN_Update_CNLF_CPL_MoW_WW46_Updated .pdf

| | | | | | |
|---|------------|--------------------|------------|---|--|
| Security Classification | | Compal Secret Data | | <div>DECLASSIFICATION/PROPRIETARY</div> <div>Compal Electronics, Inc.</div> | |
| Issued Date | 2015/12/16 | Deciphered Date | 2016/12/13 | Title | P47-PD USB TYPE-C 3 |
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| | | | | Date: | Monday, October 22, 2016 <div> <div>Sheet</div> <div>47</div> <div>of 100</div> </div> |

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| 2018/01/23 | | 2022/12/31 | | Title | |
| | | | | P048 - Reserve | |
| | | | | Size | Rev |
| | | | | Document Number | 0.1 |
| | | | | LA-E671P | |
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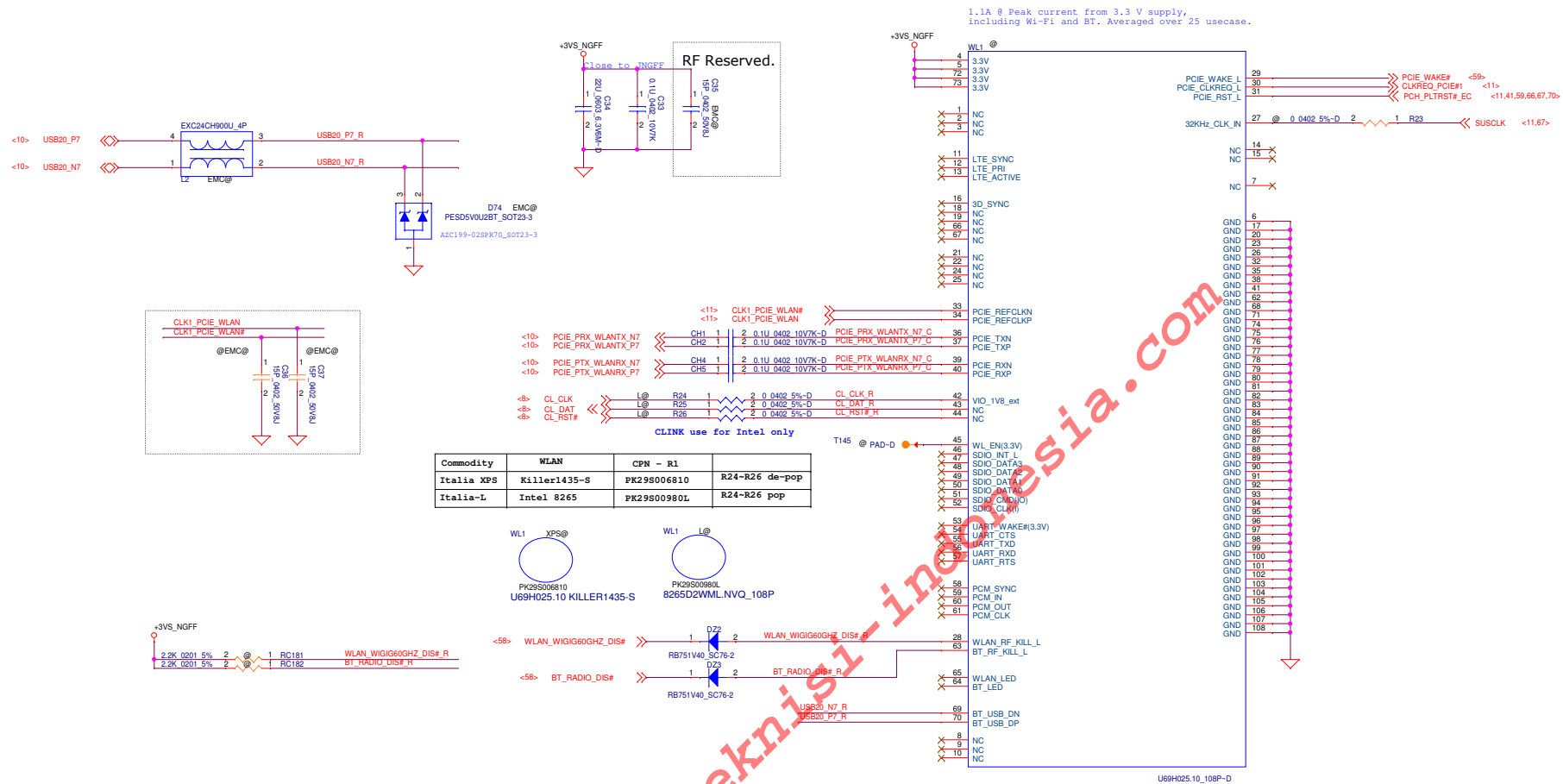
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| Security Classification | | Compal Secret Data | | DELL CONFIDENTIAL/PROPRIETARY | |
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| | | | | LA-E671P | |
| Date: | | | | Monday, October 22, 2018 | |
| Sheet | | | | 51 of 100 | |

M.2 Slot-A Key-A (WLAN)



CIS footprint change to Killer1435-S
U69H025.10_108P~D

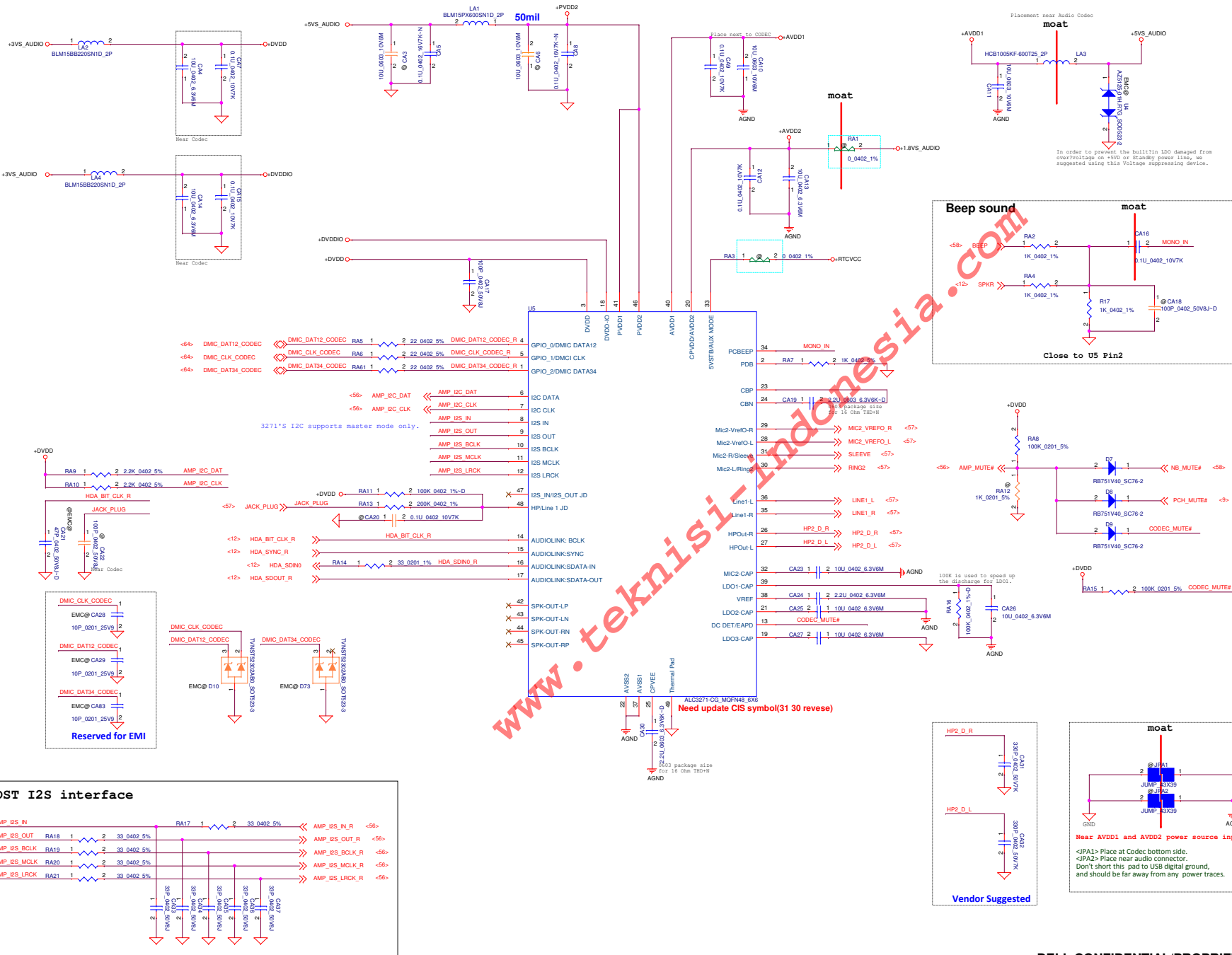
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| | | | | Document Number | 0.1 |
| Date: Monday, October 22, 2018 | | | | Sheet | 53 of 100 |

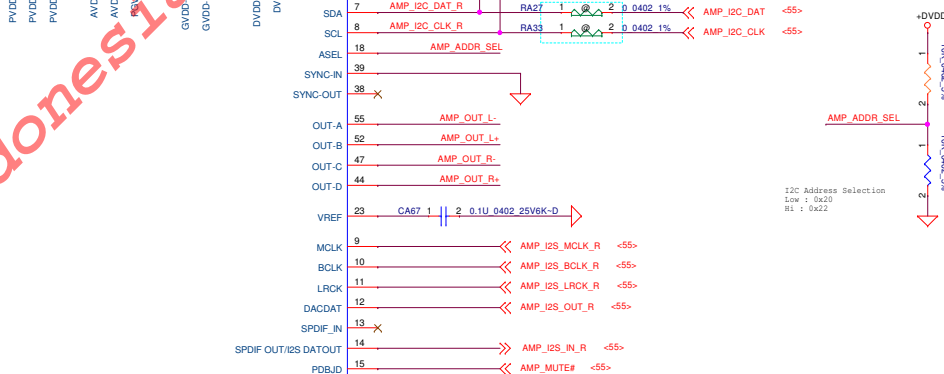
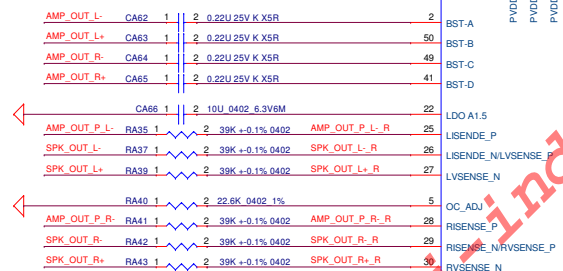
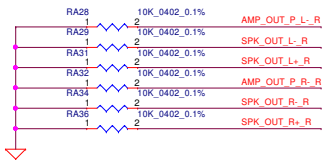
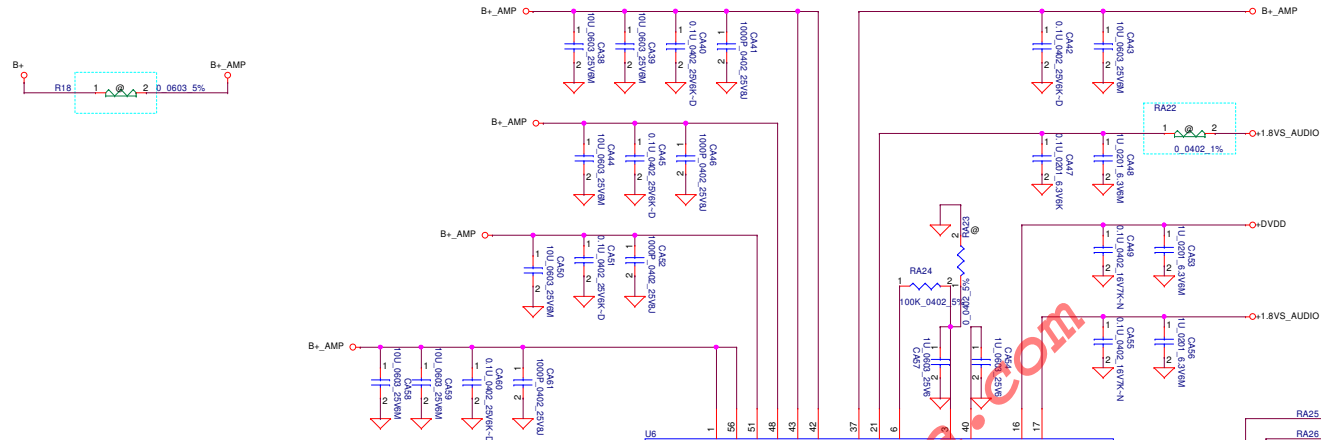
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HD Audio Codec



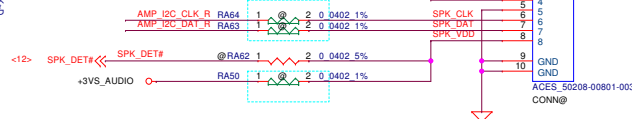
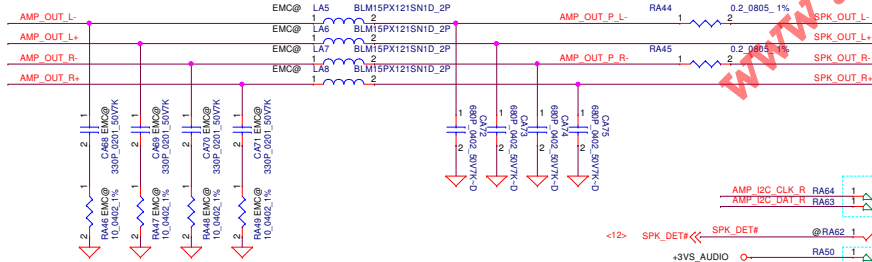
SMART AMP



Int. Speaker Conn.

Use 120 ohm bead
(SMD1000L300, MURATA BLM15PX121SN1D)

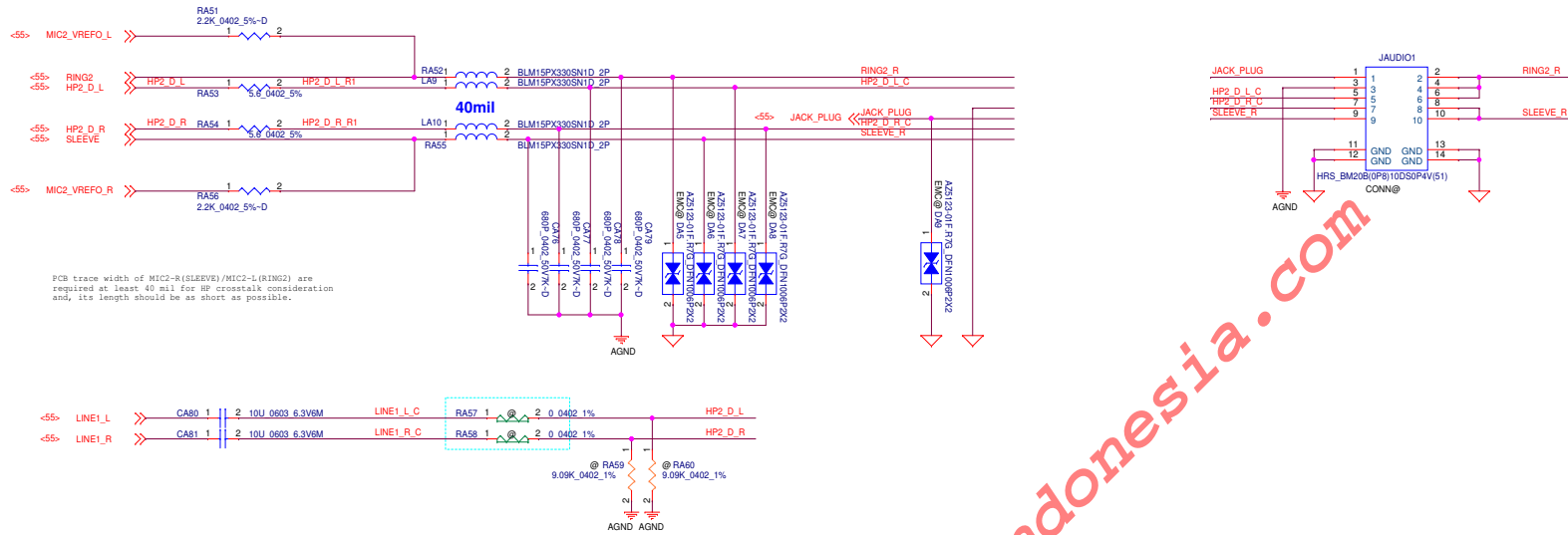
40mil = For 4ohm 3W Speaker



| Function | RA50 | RA51 |
|-------------------|-------|-------|
| EEPROM Speaker | 0 ohm | NC |
| Speaker Detection | 10K | 0 ohm |

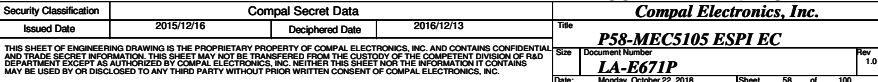
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| Security Classification | Compal Secret Data | | | DELL CONFIDENTIAL/PROPRIETARY | |
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| | | | | Size | Document Number |
| | | | | LA-E671P | |
| | | | | Rev | 1.0 |
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| | | | | Sheet | 56 of 100 |

Universal Audio Jack

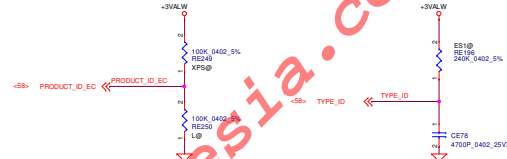
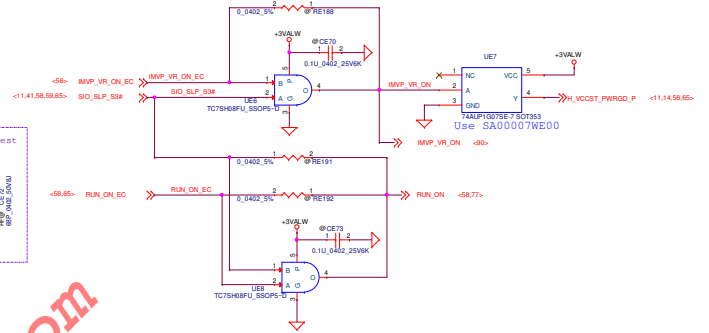
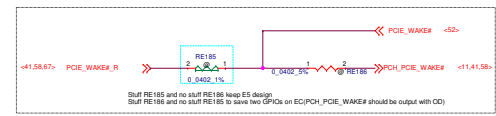
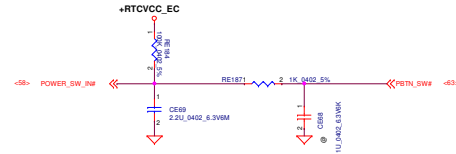
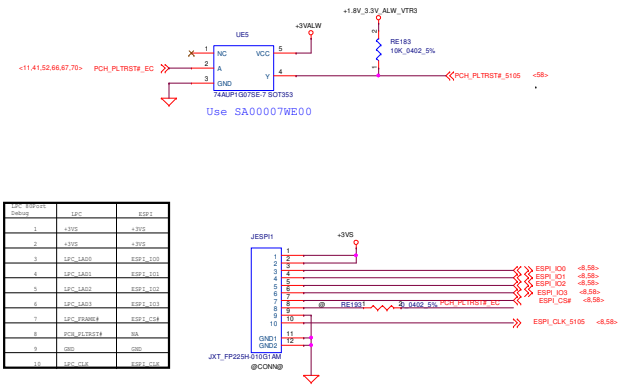


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| 2041/09/08 | | 2013/10/28 | | Title | |
| | | | | P57-Audio CONN | |
| | | | | Size | |
| | | | | LA-E671P | |
| | | | | Date | |
| | | | | Monday, October 22, 2018 | |
| | | | | Sheet | |
| | | | | 57 of 100 | |
| | | | | Rev | |
| | | | | 1.0 | |



| QFN Pinout (mm) | QFN | QFN |
|-----------------|---------|---------|
| 1 | VDD | VDD |
| 2 | VDD | VDD |
| 3 | VDD-VDD | VDD-VDD |
| 4 | VDD-VDD | VDD-VDD |
| 5 | VDD-VDD | VDD-VDD |
| 6 | VDD-VDD | VDD-VDD |
| 7 | VDD-VDD | VDD-VDD |
| 8 | VDD-VDD | VDD-VDD |
| 9 | VDD-VDD | VDD-VDD |
| 10 | VDD-VDD | VDD-VDD |

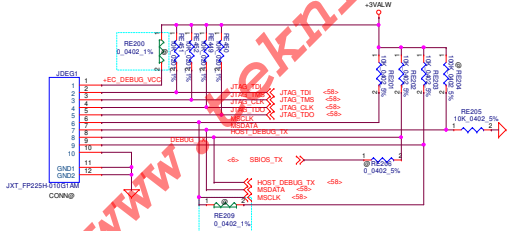


| RE249 | RE250 | REV |
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| @ | @ | Italia XPS |
| @ | @ | Italia |

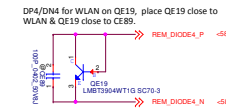
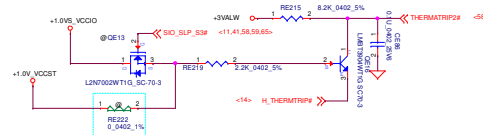
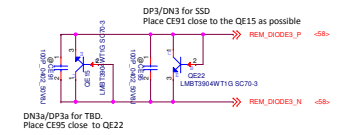
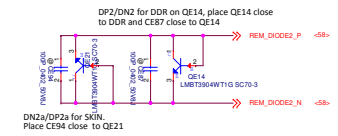
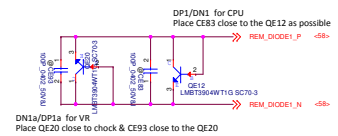
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| 130K | 4700p | ES2 |
| 62K | 4700p | QS |
| 33K | 4700p | U22 |
| 8.2K | 4700p | V-PRO |
| 4.3K | 4700p | . |
| 2K | 4700p | . |
| 1K | 4700p | . |

| RE194 | CE75 | REV |
|-------|-------|-----|
| 240K | 4700p | X00 |
| 130K | 4700p | X01 |
| 62K | 4700p | X02 |
| 33K | 4700p | X03 |
| 8.2K | 4700p | X04 |
| 4.3K | 4700p | A00 |
| 2K | 4700p | . |
| 1K | 4700p | . |

| RE195 | CE76 | PANEL SIZE |
|-------|-------|---------------|
| 240K | 4700p | |
| 130K | 4700p | |
| 33K | 4700p | |
| 4.3K | 4700p | Italia 13 WHL |



| Thermal diode mapping | 5105 Channel | Location |
|-----------------------|--------------|----------------|
| DP1/DN1 | OTP (QE12) | |
| SEN4 | DN1a/DP1a | Charger (QE20) |
| SEN1 | DP2/DN2 | DDR (QE14) |
| SEN5 | DN2a/DP2a | SKIN (QE21) |
| SEN6 | DP3/DN3 | SKIN (QE22) |
| SEN2 | DN3a/DP3a | SSD (QE15) |
| SEN3 | DP4/DN4 | WLAN (QE19) |
| | DN4a/DP4a | |



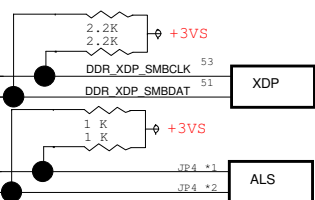
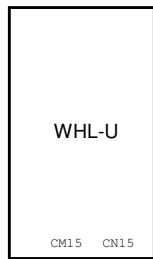
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.

| Security Classification | Compal Secret Data | Deciphered Date | 2016/12/13 |
|-------------------------|--------------------|-----------------|------------|
| Issued Date | 2016/12/16 | Deciphered Date | 2016/12/13 |

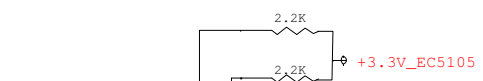
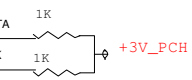
P59-MEC5105 Support
LA-E671P

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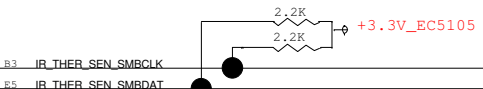
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| Security Classification | | Compal Secret Data | | DELL CONFIDENTIAL/PROPRIETARY | |
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| | | | | P060 - Reserve | |
| | | | | Document Number | |
| Date: Monday, October 22, 2018 | | | | Rev 0-1(000) | |
| Sheet 60 of 100 | | | | LA-E671P | |



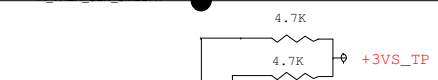
ALS address selection 0x52_TBD
Sensor address selection 0x6C_TBD



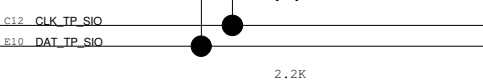
TI PD address selection 0x70_TBD
PD_Debug address selection 0xEC_TBD



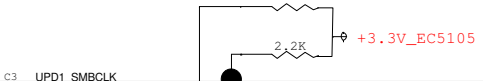
IR_THER_S



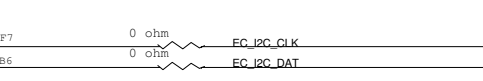
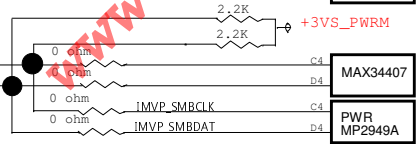
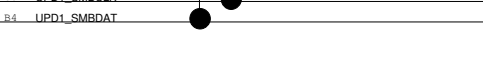
TP address :0x42_TBD



PD_Debug address selection 0xEC_TBD
TI PD address selection 0x70_TBD



I2C address selection L= 0x20H (L= 0x20H ; H= 0x22H)_TBD



TI PD3



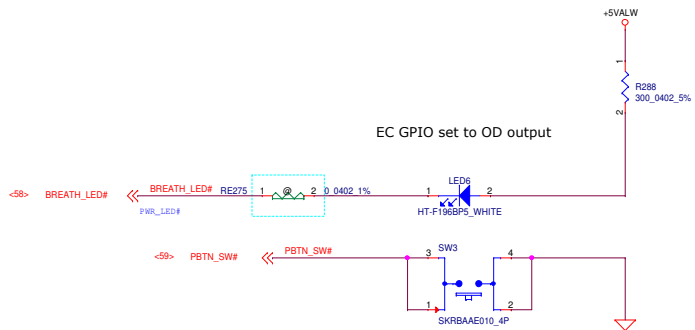
Battery address selection 0x16_TBD
Charger address selection 0x12_TBD



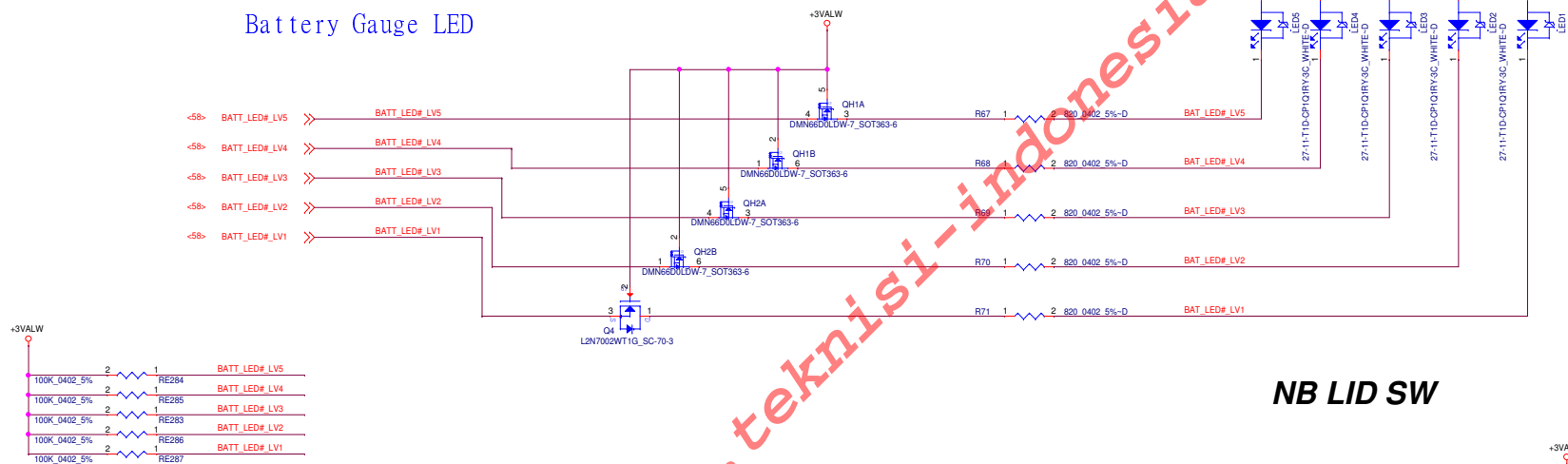
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| | | | | Size | Document Number | Rev |
| | | | | LA-E671P | | 0.1 |
| | | | | Date: | Monday, October 22, 2018 | Sheet |
| | | | | | 62 | of |

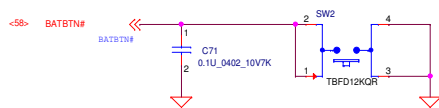
Power Button +LED



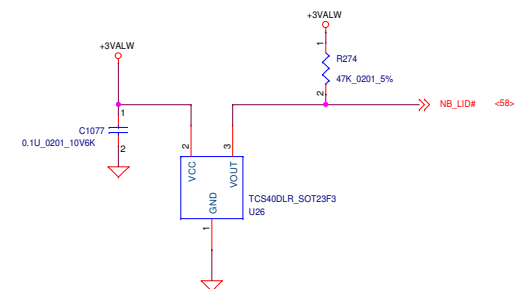
Battery Gauge LED



Battery Gauge Button



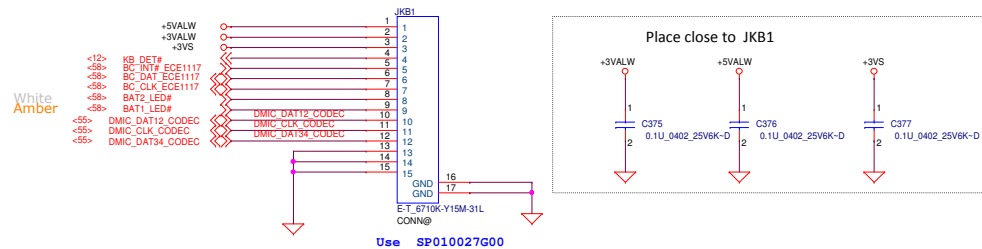
NB LID SW



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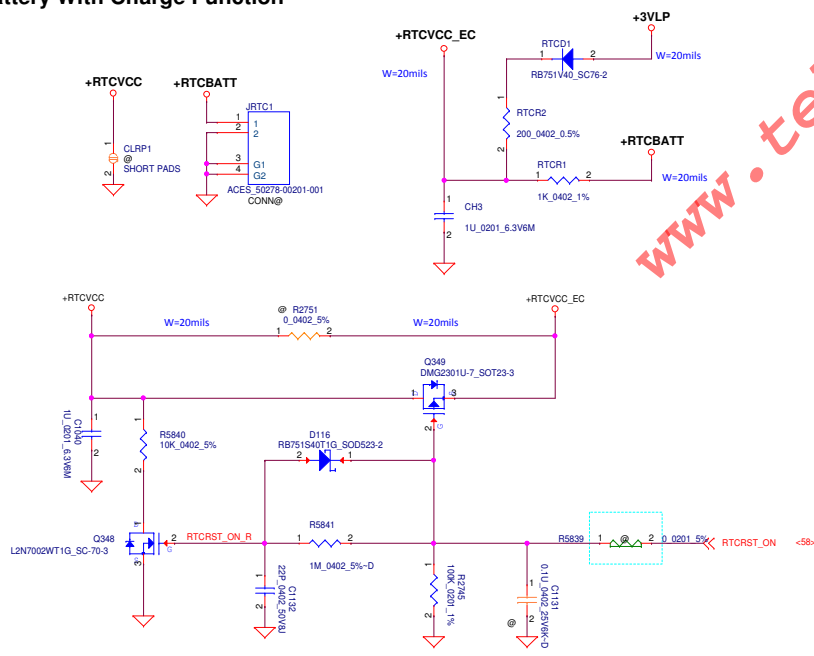
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| | | | | P63-Battery LED / LID | |
| | | | | Size Document Number LA-E671P | |
| | | | | Date: Monday, October 22, 2018 Sheet 63 of 100 | |

Keyboard Controller board + DMIC

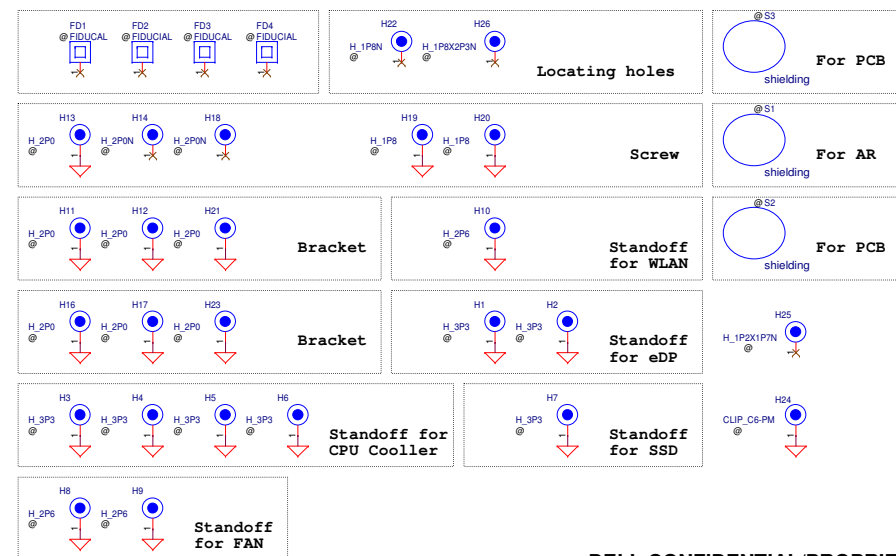


Power Monitor

RTC Battery With Charge Function



SCREW Hole

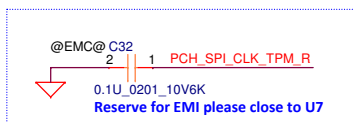
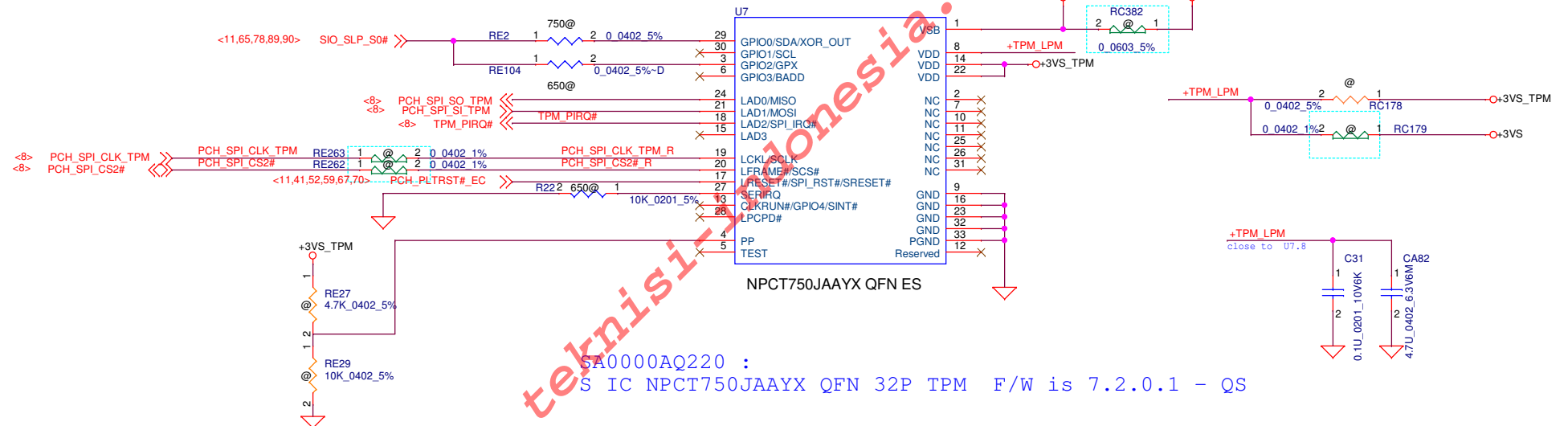
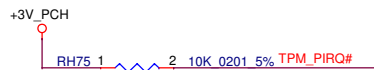
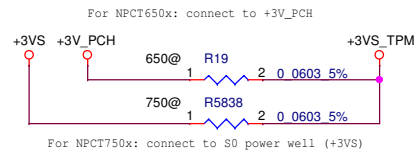


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| Issued Date | | Deciphered Date | | Compal Electronics, Inc. | |
| 2015/12/16 | | 2016/12/13 | | Title | |
| | | | | P64-SCREWH/KB/RTC/IR T/PWRM | |
| | | | | Size | |
| | | | | LA-E671P | |
| | | | | Date | |
| | | | | Monday, October 22, 2018 | |
| | | | | Sheet | |
| | | | | 64 of 100 | |
| | | | | Rev | |
| | | | | 1.0 | |

NOTE:
Follow the SPI topology layout guidelines
in the relevant Intel Platform Design Guide

TPM

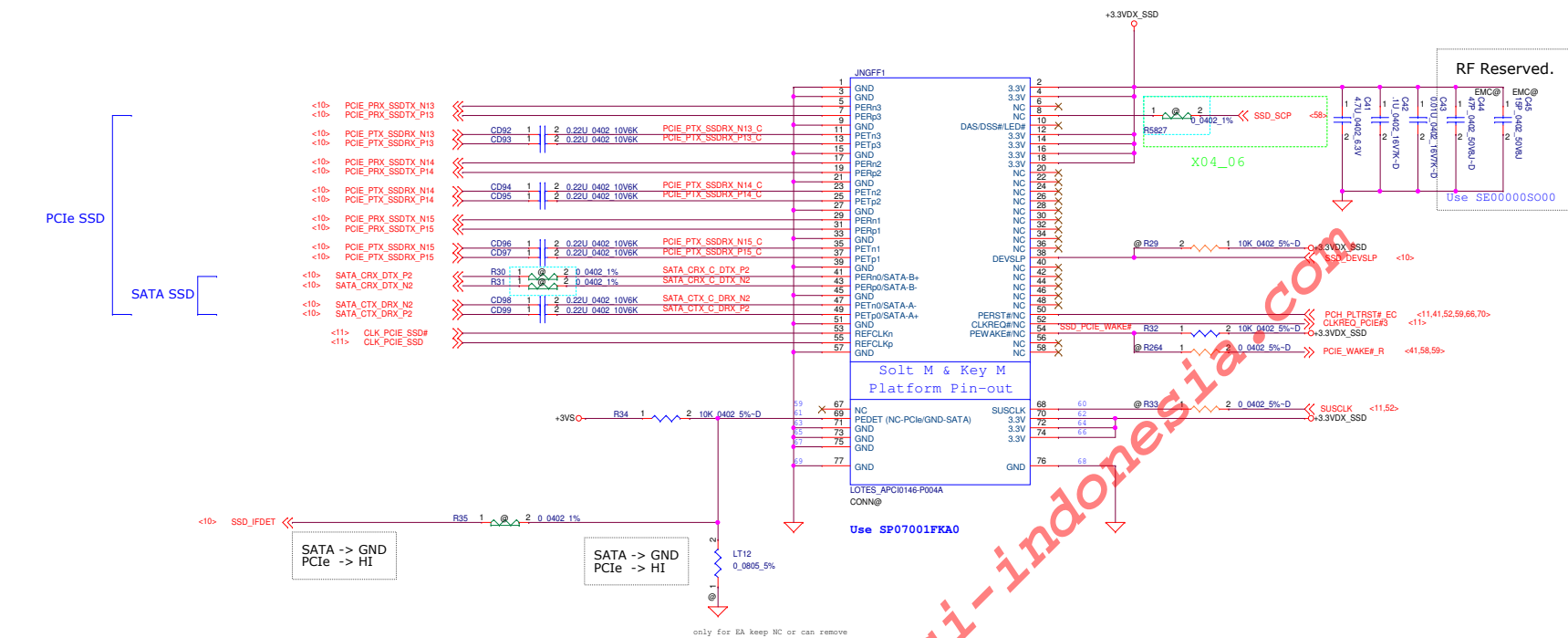
NOTE:
Place 0.1 uF capacitors as close as
possible to the device power pins



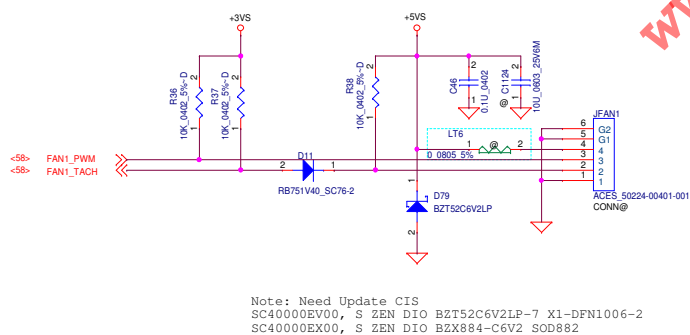
- Pin14&Pin22 (+3VS_TPM):
For NPCT650x: connect to same power well with host SPI interface (it should be +3V_PCH)
For NPCT750x: connect to S0 power well (+3VS)
- Pin27:
For NPCT650x: pop R22
For NPCT750x: de-pop R22
- SLP_S0# connection:
For NPCT650x: pop RE104, de-pop RE2
For NPCT750x: pop RE2, de-pop RE104
- RC180 can be just deleted for both NPCT650x and NPCT750x
- TPM_PIRQ# is recommended that pull-up to same GPIO power well at host side

| | | | | | |
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| | | | | Document Number | |
| | | | | LA-E671P | |
| | | | | Rev | |
| | | | | 1.0 | |
| | | | | Date: Monday, October 22, 2018 | |
| | | | | Sheet 66 of 100 | |

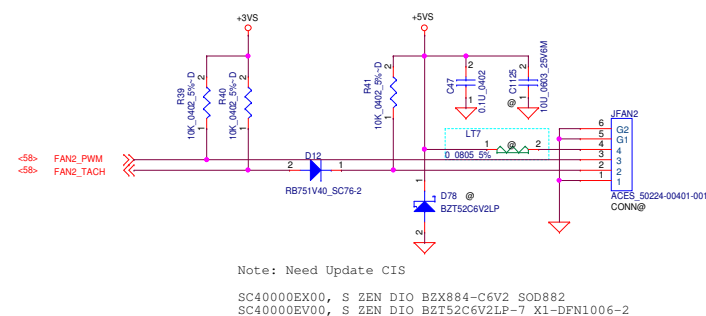
M.2 Slot-C Key-M (SSD)



FAN 1



FAN 2



| | | | | | |
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| Size | | Document Number | | LA-E671P | |
| C | | Date | | Monday, October 22, 2018 | |
| Sheet | | 67 | | of | |
| 100 | | | | | |

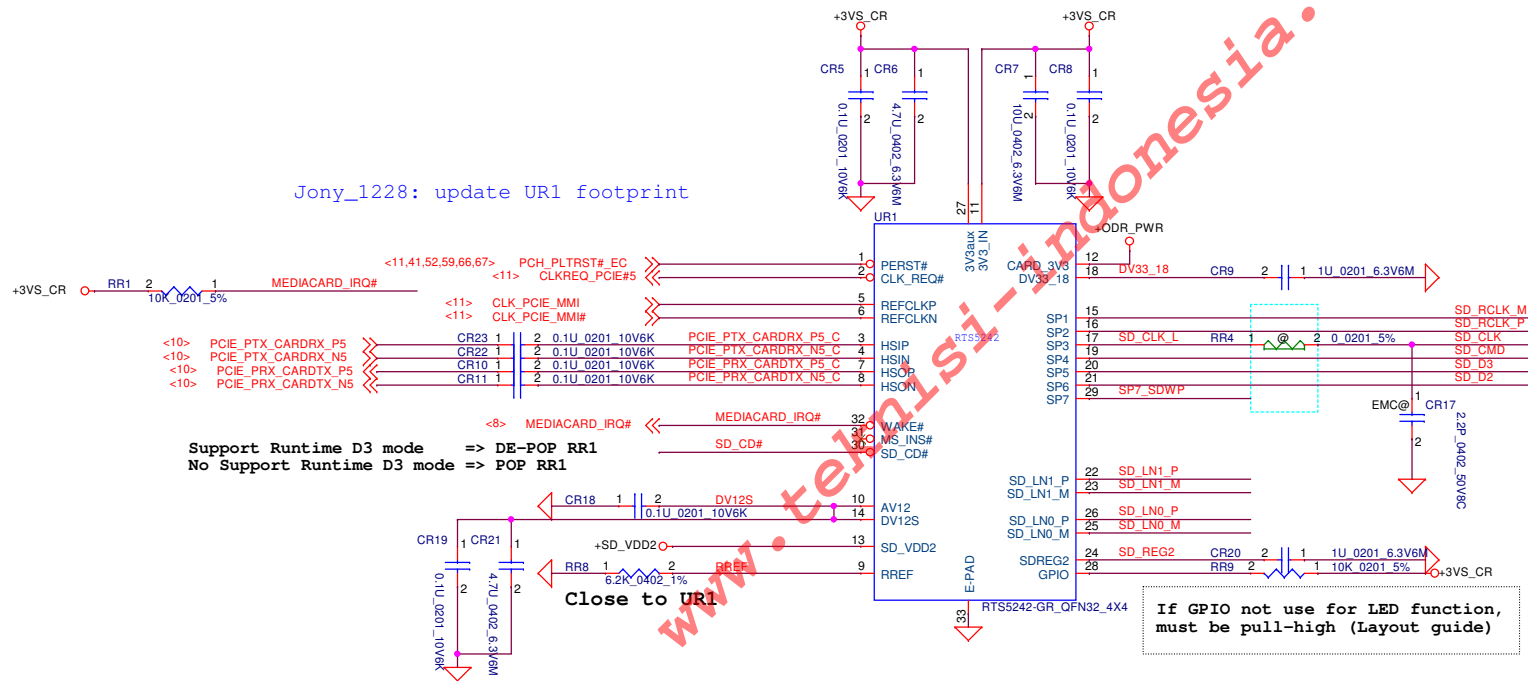
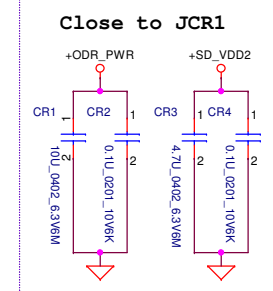
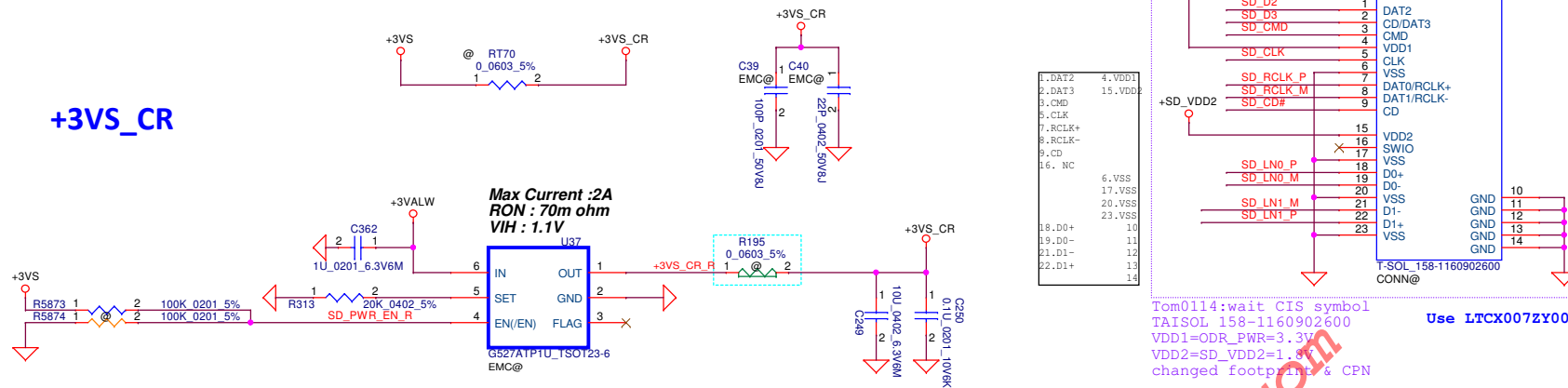
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| | | | | Date Monday, October 22, 2018 | Sheet 68 of 100 |

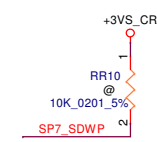
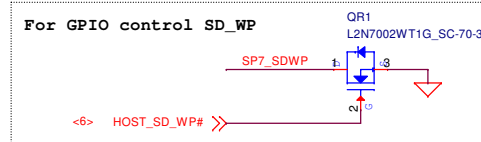
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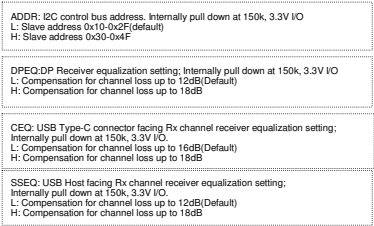
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| | | | | Date Monday, October 22, 2018 | Sheet 69 of 100 |

Card Reader



- 1) Placing the RTS5242 chip and flash card socket locate to suit trace routing for SI / EMI / ESD.
- 2) Keep bulk and de-coupling capacitors as close as possible to the RTS5242 chip and flash card socket.
 - Bulk capacitor for Card_3V3 place closed to flash card socket.
 - Bulk capacitor for 3V3_IN / 3V3aux / DV12S place closed to RTS5242 chip.
- 3) Keep damping resistor (ex, for SD CLK / MS CLK) as close as possible to the RTS5242 chip.
- 4) Keep these capacitors for SD card / MS card signals as close as possible to flash card socket.





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| Title | P071-DP/USB3 Repeater SW2 PS8802 | | |
| Size B | Document Number | Rev | |
| | LA-E671P | 0.2 | |
| Date: | Monday, October 22, 2018 | Sheet | 71 of 100 |

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| | | | | Date: Monday, October 22, 2018 | | | | |
| | | | | Sheet | | 72 of 100 | | |

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| | | | | P073 - Reserve | |
| | | | | Size | Rev |
| | | | | Document Number | 0.1 |
| | | | | LA-E671P | |
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| | | | | Sheet | 73 of 100 |

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| | | | | Date Monday, October 22, 2018 | Sheet 74 of 100 |

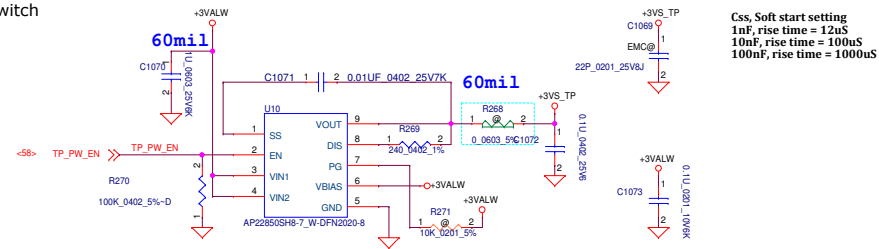
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| | | | | Date Monday, October 22, 2018 | Sheet 75 of 100 |

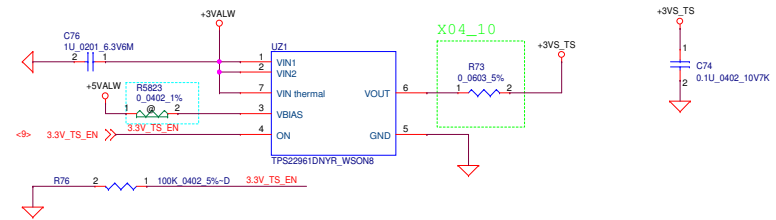
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| | | | | Sheet | 76 of 100 |
| | | | | Rev | 0.1 |
| | | | | LA-E671P | |

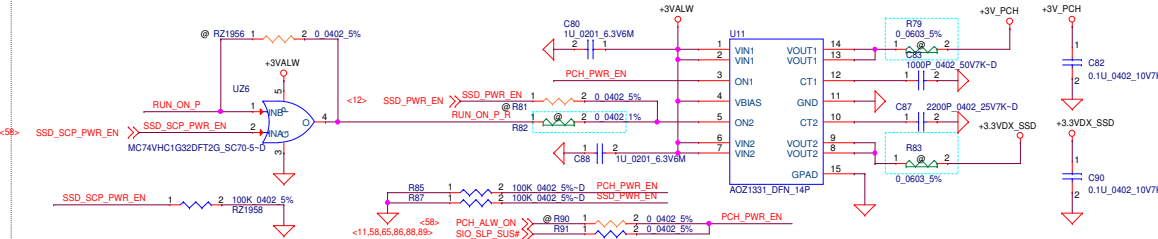
Touch Pad Load Switch



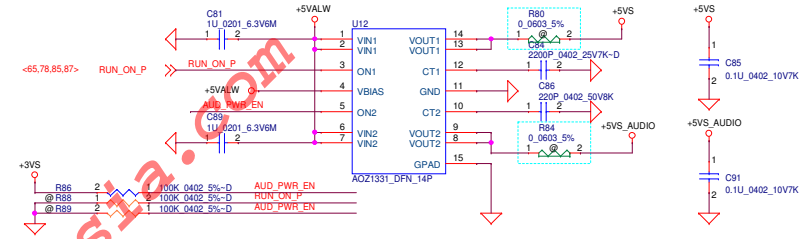
Touch Screen Load Switch



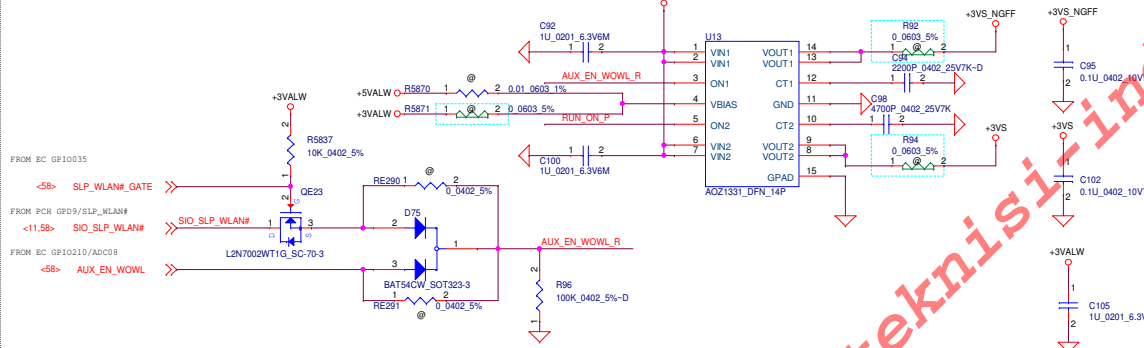
Deeper Sleep, SSD Load Switch



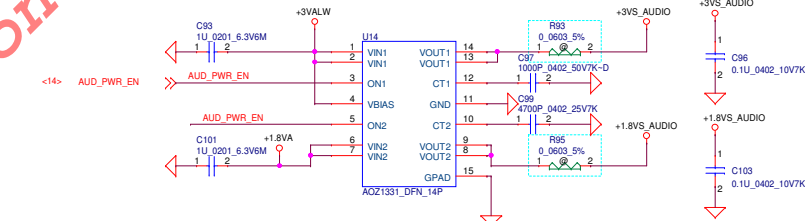
5V_Run, 5V_Audio Load Switch



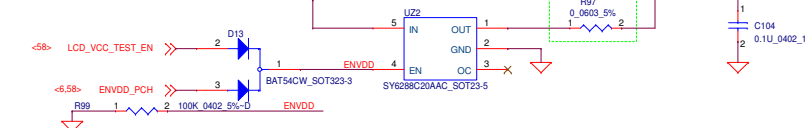
WiFi, 3V_RUN Load Switch



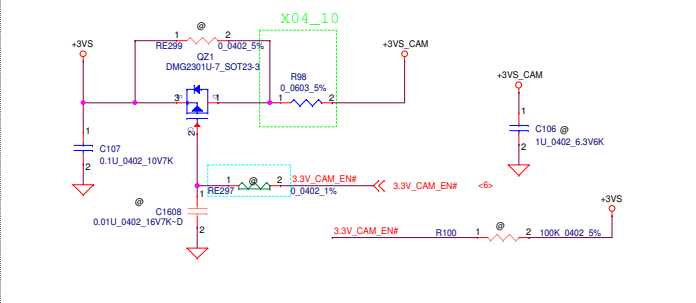
3V_Audio, 1.8V_Audio Load Switch



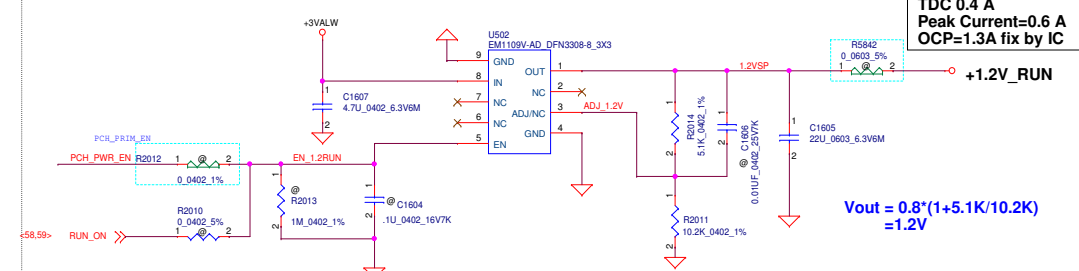
LCD Load Switch



Camera

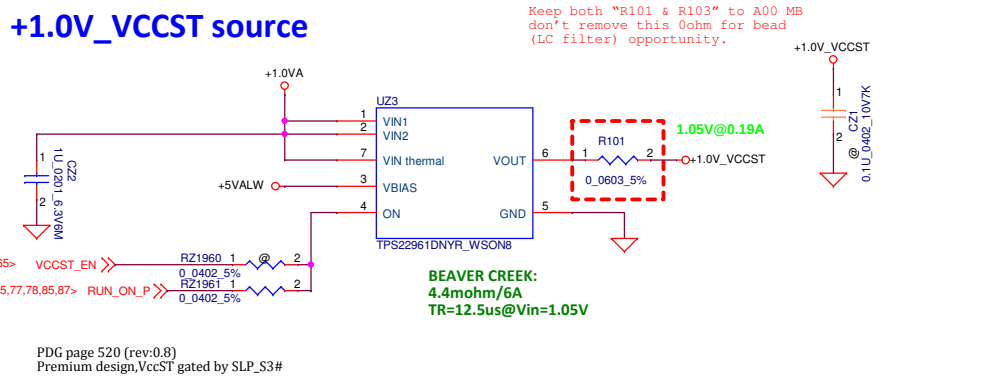


TypeC-SW MUX Load Switch

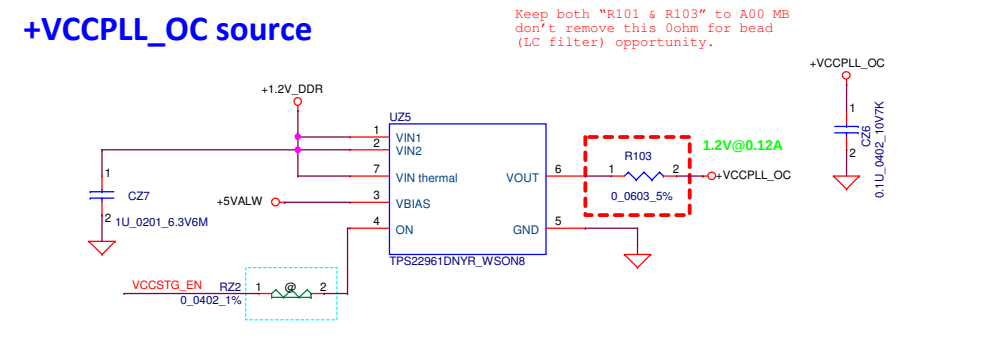


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| | | P77-DC/DC Interface 1 |
| | | Size |
| | | Document Number |
| | | LA-E671P |
| | | Date |
| | | Monday, October 22, 2018 |
| | | Sheet |
| | | 77 of 100 |

+1.0V_VCCST source

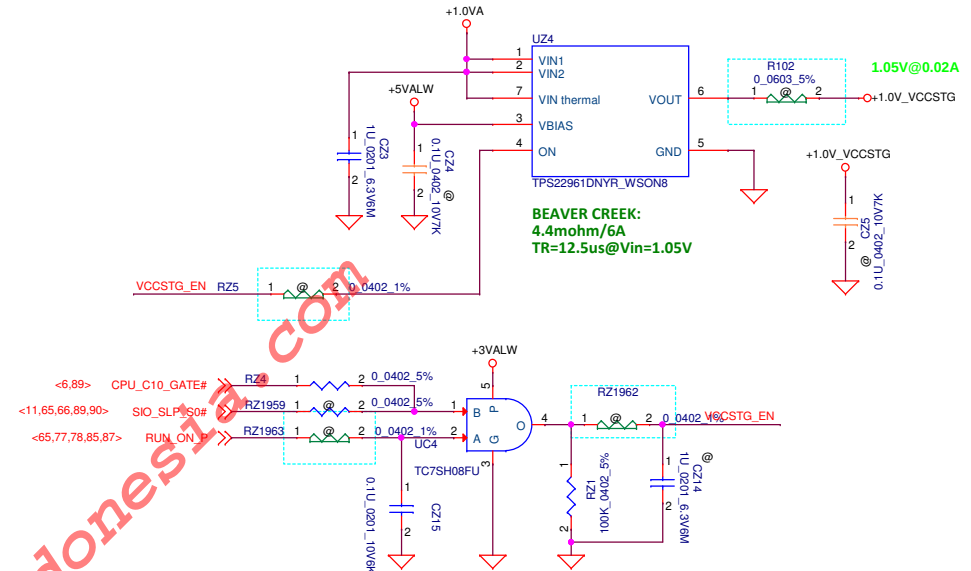


+VCCPLL_OC source



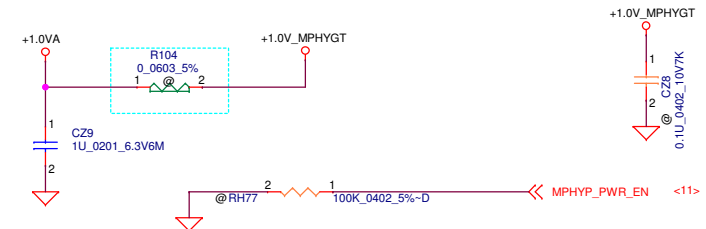
+1.8VU Load Switch

+1.0V_VCCSTG source



| | S0 | S0Ix | S3 |
|-------------|------|------|-----|
| SIO_SLP_S0# | high | low | low |
| RUN_ON_EC | high | high | low |










+1.0V_MPHYGT source



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| | | | | Date Monday, October 22, 2018 | Sheet 79 of 100 |


4+2 CPU Option

| | | | | |
|---|--|--|--|--|
| UCPU1 ES1_4+2@  SA0000BX10L SA0000BX10L_ES1 | UCPU1 QS@  SA0000C6R1L I3-8145U_2.1G | UCPU1 QS@  SA0000C6O1L I5-8265U_1.6G | UCPU1 VPRO@  SA0000CF10L I7-8565U_1.8G | UCPU1 VPRO@  SA0000C611L I5-8265U_1.6G |
| UCPU1 ES2_4+2@  BBBBBB ZZZZZZZZ | UCPU1 QS@  SA0000C6P2L I7-8565U_1.8G | UCPU1 QS@  SA0000C6Q3L I5-8265U_1.6G | UCPU1 QS@  SA0000C6Q3L I3-8145U_2.1G | |

AR Option

| |
|--|
| UT2 AR_SLL42@  SA0000ZV3L DSL6340 SLL42 B2 |
|--|

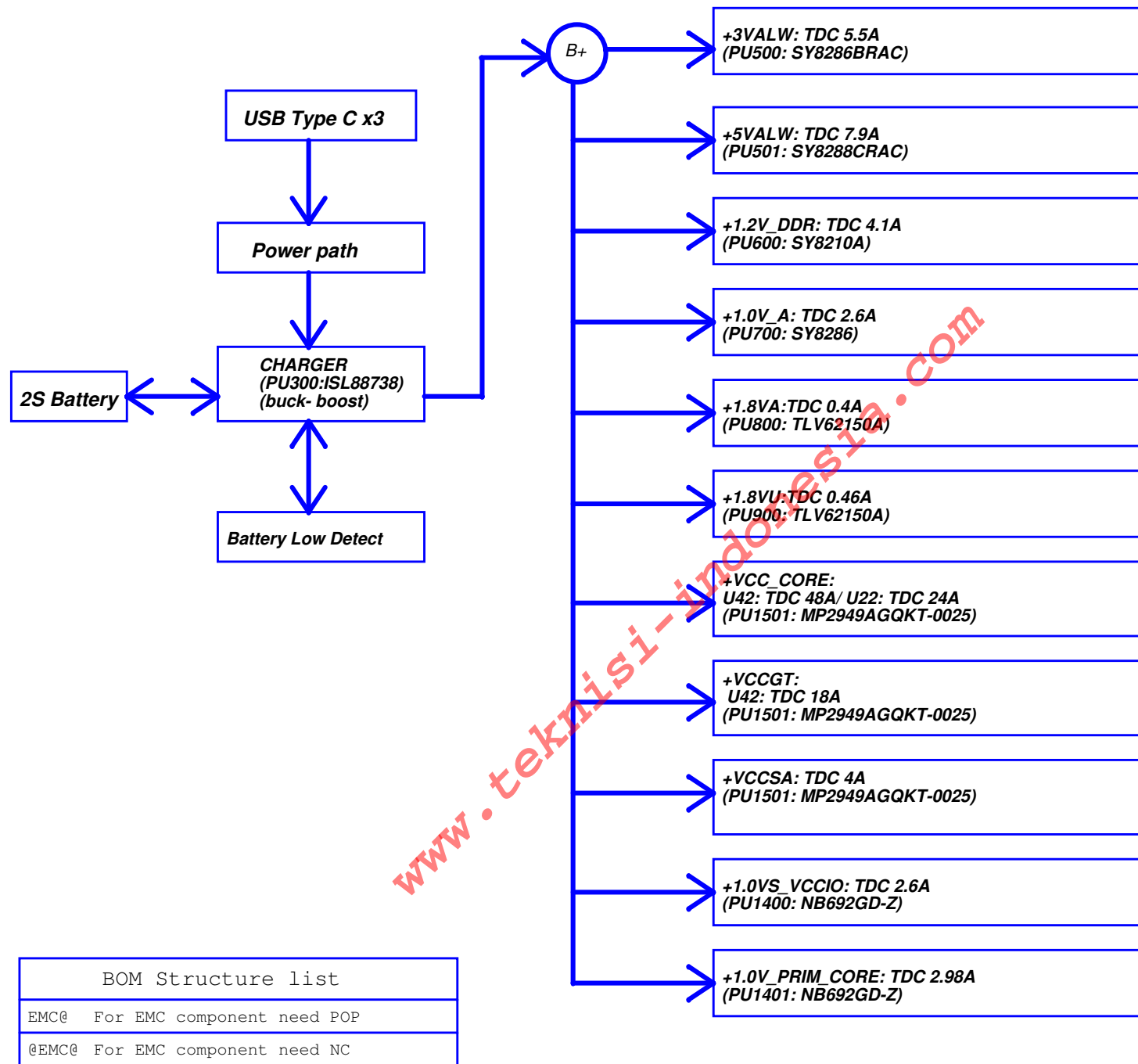
TPM Option

| |
|---|
| U7 TPM750@  SA0000AQ220 TPM750 - QS FW is 7.2.0.1 |
|---|

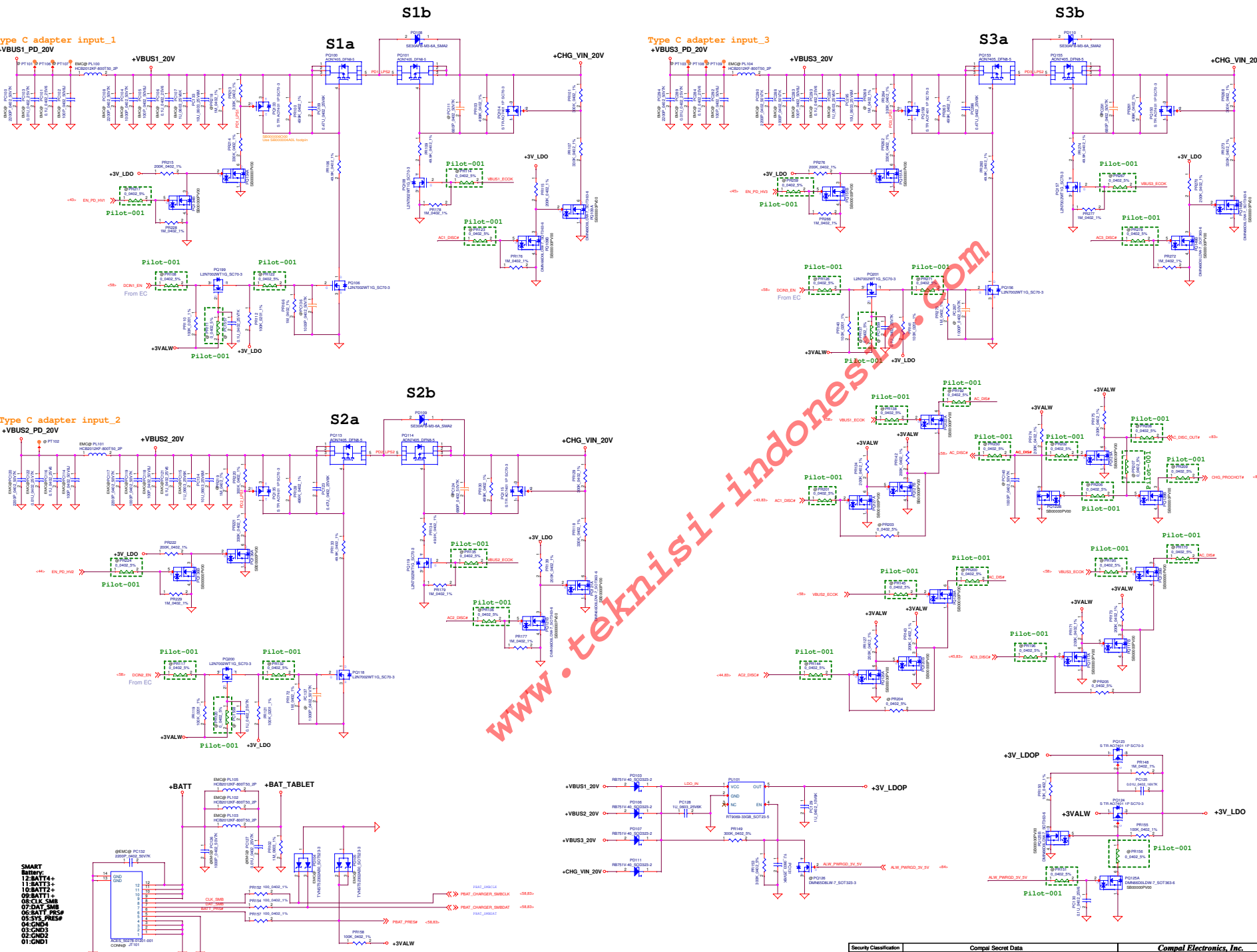
DRAM Option

DRAM Config Option

| | | | | | | | | | |
|---|---|---|---|---|--|--|--|--|--|
| Micron 4G/2133 SA0000AZU0L MT52L256M32D1PF-093 WT:B MT52L256M32D1PF-093 WT:B MT52L256M32D1PF-093 WT:B MT52L256M32D1PF-093 WT:B | UD1 M4G_2133@  | UD2 M4G_2133@  | UD3 M4G_2133@  | UD4 M4G_2133@  | MEM_CONFIG0 RH51 M4G_2133@  SD028100280 10K_0402_5% | MEM_CONFIG1 RH54 M4G_2133@  SD028100280 10K_0402_5% | MEM_CONFIG2 RH56 M4G_2133@  SD028100280 10K_0402_5% | MEM_CONFIG3 RH57 M4G_2133@  SD028100280 10K_0402_5% | MEM_CONFIG4 RH60 M4G_2133@  SD028100280 10K_0402_5% |
| Micron 8G/2133 SA00009U70L MT52L512M32D2PF-093 WT:B MT52L512M32D2PF-093 WT:B MT52L512M32D2PF-093 WT:B MT52L512M32D2PF-093 WT:B | UD1 M8G_2133@  | UD2 M8G_2133@  | UD3 M8G_2133@  | UD4 M8G_2133@  | RH52 M8G_2133@  SD028100280 10K_0402_5% | RH53 M8G_2133@  SD028100280 10K_0402_5% | RH56 M8G_2133@  SD028100280 10K_0402_5% | RH57 M8G_2133@  SD028100280 10K_0402_5% | RH60 M8G_2133@  SD028100280 10K_0402_5% |
| Micron 16G/2133 SA000092N0L MT52L1G32D4PG-093WT:B MT52L1G32D4PG-093WT:B MT52L1G32D4PG-093WT:B MT52L1G32D4PG-093WT:B | UD1 M16G_2133@  | UD2 M16G_2133@  | UD3 M16G_2133@  | UD4 M16G_2133@  | RH52 M16G_2133@  SD028100280 10K_0402_5%-D | RH54 M16G_2133@  SD028100280 10K_0402_5%-D | RH56 M16G_2133@  SD028100280 10K_0402_5%-D | RH58 M16G_2133@  SD028100280 10K_0402_5%-D | RH59 M16G_2133@  SD028100280 10K_0402_5%-D |
| Samsung 4G/2133 SA0000BTE0L K4E8E324EB-EGCG K4E8E324EB-EGCG K4E8E324EB-EGCG K4E8E324EB-EGCG | UD1 S4G_2133@  | UD2 S4G_2133@  | UD3 S4G_2133@  | UD4 S4G_2133@  | RH51 S4G_2133@  SD028100280 10K_0402_5%-D | RH53 S4G_2133@  SD028100280 10K_0402_5%-D | RH55 S4G_2133@  SD028100280 10K_0402_5%-D | RH57 S4G_2133@  SD028100280 10K_0402_5%-D | RH60 S4G_2133@  SD028100280 10K_0402_5%-D |
| Samsung 8G/1866 SA0000A2T1L K4E6E304EC-EGCG K4E6E304EC-EGCG K4E6E304EC-EGCG K4E6E304EC-EGCG | UD1 S8G_2133@  | UD2 S8G_2133@  | UD3 S8G_2133@  | UD4 S8G_2133@  | RH52 S8G_2133@  SD028100280 10K_0402_5%-D | RH54 S8G_2133@  SD028100280 10K_0402_5%-D | RH56 S8G_2133@  SD028100280 10K_0402_5%-D | RH58 S8G_2133@  SD028100280 10K_0402_5%-D | RH59 S8G_2133@  SD028100280 10K_0402_5%-D |
| Samsung 16G/2133 SA00008VV2L K4EBE304EC-EGCG K4EBE304EC-EGCG K4EBE304EC-EGCG K4EBE304EC-EGCG | UD1 S16G_2133@  | UD2 S16G_2133@  | UD3 S16G_2133@  | UD4 S16G_2133@  | RH52 S16G_2133@  SD028100280 10K_0402_5%-D | RH53 S16G_2133@  SD028100280 10K_0402_5%-D | RH56 S16G_2133@  SD028100280 10K_0402_5%-D | RH57 S16G_2133@  SD028100280 10K_0402_5%-D | RH59 S16G_2133@  SD028100280 10K_0402_5%-D |
| Hynix 4G/2133 SA0000AZR0L H9CCNN8GTALAR-NVD H9CCNN8GTALAR-NVD H9CCNN8GTALAR-NVD H9CCNN8GTALAR-NVD | UD1 H4G_2133@  | UD2 H4G_2133@  | UD3 H4G_2133@  | UD4 H4G_2133@  | RH52 H4G_2133@  SD028100280 10K_0402_5%-D | RH54 H4G_2133@  SD028100280 10K_0402_5%-D | RH56 H4G_2133@  SD028100280 10K_0402_5%-D | RH57 H4G_2133@  SD028100280 10K_0402_5%-D | RH60 H4G_2133@  SD028100280 10K_0402_5%-D |
| Hynix 8G/2133 SA0000ALP0L H9CCNN8BTALAR-NUD H9CCNN8BTALAR-NUD H9CCNN8BTALAR-NUD H9CCNN8BTALAR-NUD | UD1 H8G_2133@  | UD2 H8G_2133@  | UD3 H8G_2133@  | UD4 H8G_2133@  | RH51 H8G_2133@  SD028100280 10K_0402_5%-D | RH54 H8G_2133@  SD028100280 10K_0402_5%-D | RH56 H8G_2133@  SD028100280 10K_0402_5%-D | RH57 H8G_2133@  SD028100280 10K_0402_5%-D | RH60 H8G_2133@  SD028100280 10K_0402_5%-D |
| Hynix 16G/2133 SA000092L0L H9CCNN8GLALAR-NVD H9CCNN8GLALAR-NVD H9CCNN8GLALAR-NVD H9CCNN8GLALAR-NVD | UD1 H16G_2133@  | UD2 H16G_2133@  | UD3 H16G_2133@  | UD4 H16G_2133@  | RH51 H16G_2133@  SD028100280 10K_0402_5%-D | RH53 H16G_2133@  SD028100280 10K_0402_5%-D | RH56 H16G_2133@  SD028100280 10K_0402_5%-D | RH58 H16G_2133@  SD028100280 10K_0402_5%-D | RH59 H16G_2133@  SD028100280 10K_0402_5%-D |

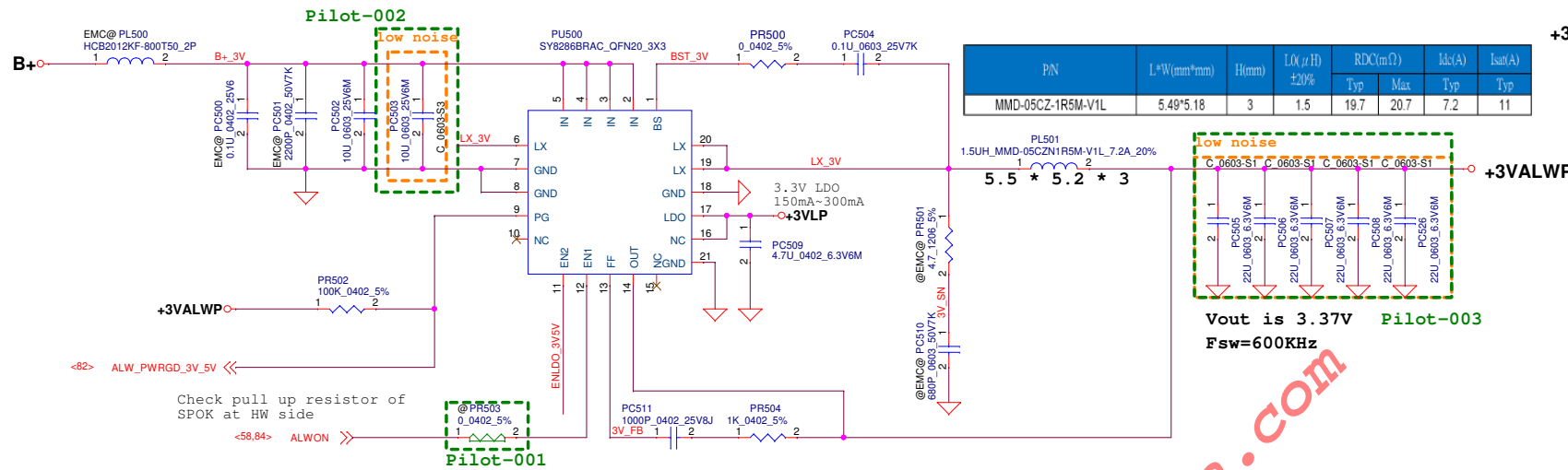


Function feild :
Power Path(37.1) , EMC Part(47.1)



SMART
Battery:
12-BATT+
11-BATT3+
10-BATT2+
09-BATT1+
08-BATT+
07-BATT-
06-BATT_PRES#
05-BATT_PRES#
04-BATT_PRES#
03-BATT_PRES#
02-BATT_PRES#
01-BATT_PRES#

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| LA-E672P | | LA-E672P |



+3VALWP

@ PJP500 JUMP 43X118

+3VALW

3VALWP
TDC 5.2A
Peak Current 7.5A
OCP Current 8.0A (fix)

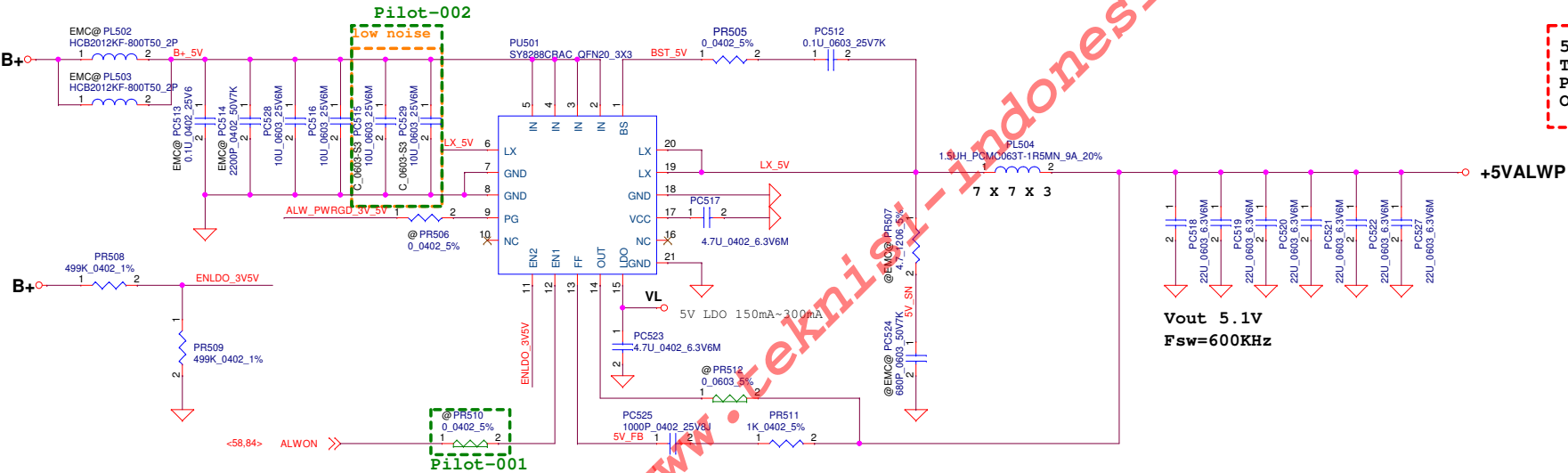
Non AR
3VALWP
TDC 5.5A
Peak Current 7.5A
OCP Current 8.0A (fix)

+5VALWP

@ PJP501 JUMP 43X118

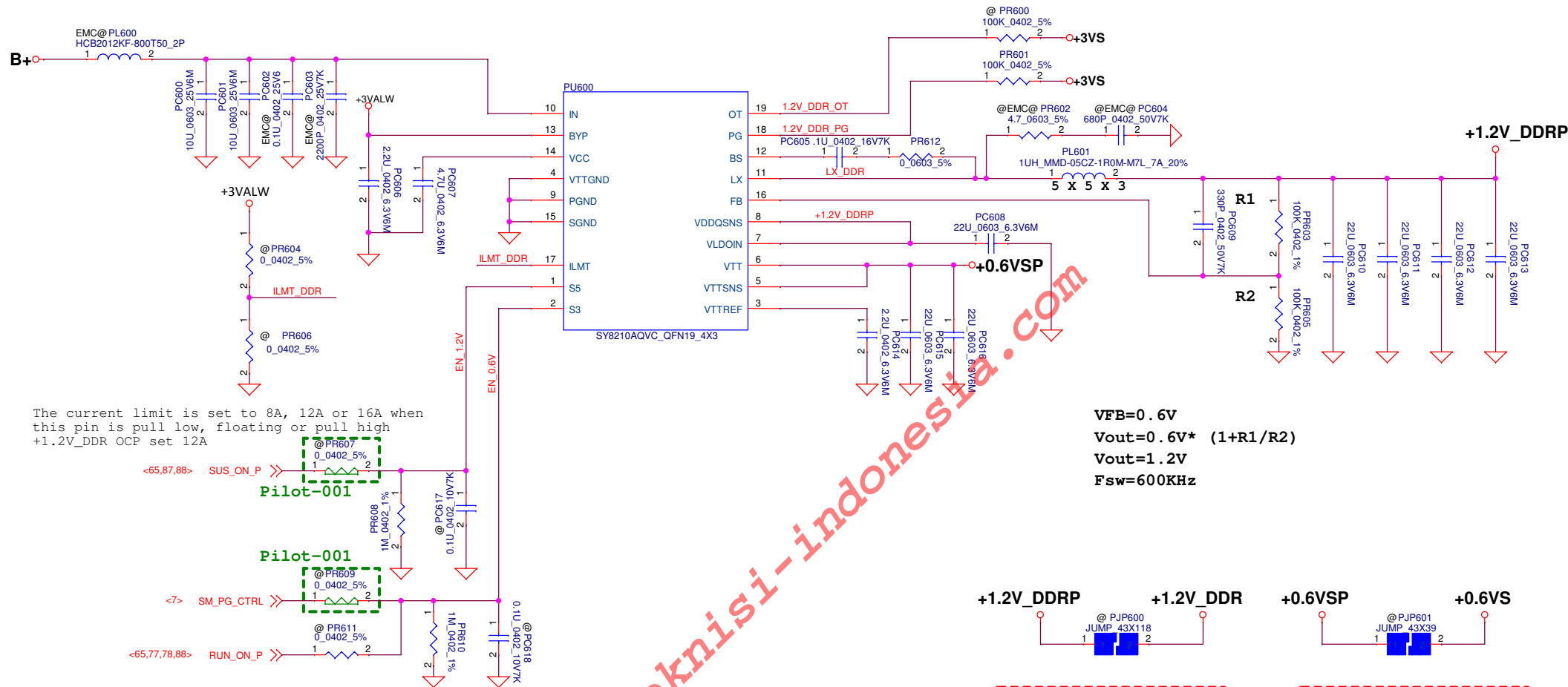
+5VALW

5VALWP
TDC 7.9A
Peak Current 11.0A
OCP Current 13.0A



3V/5V controller(35.1), Support component(35.2)

| | | | | | | |
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| | | | | Date: | Monday, October 22, 2018 | Sheet 84 of 100 |



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high +1.2V_DDR OCP set 12A

VFB=0.6V
Vout=0.6V* (1+R1/R2)
Vout=1.2V
Fsw=600KHz

DDR controller(35.3), Support component(35.4)

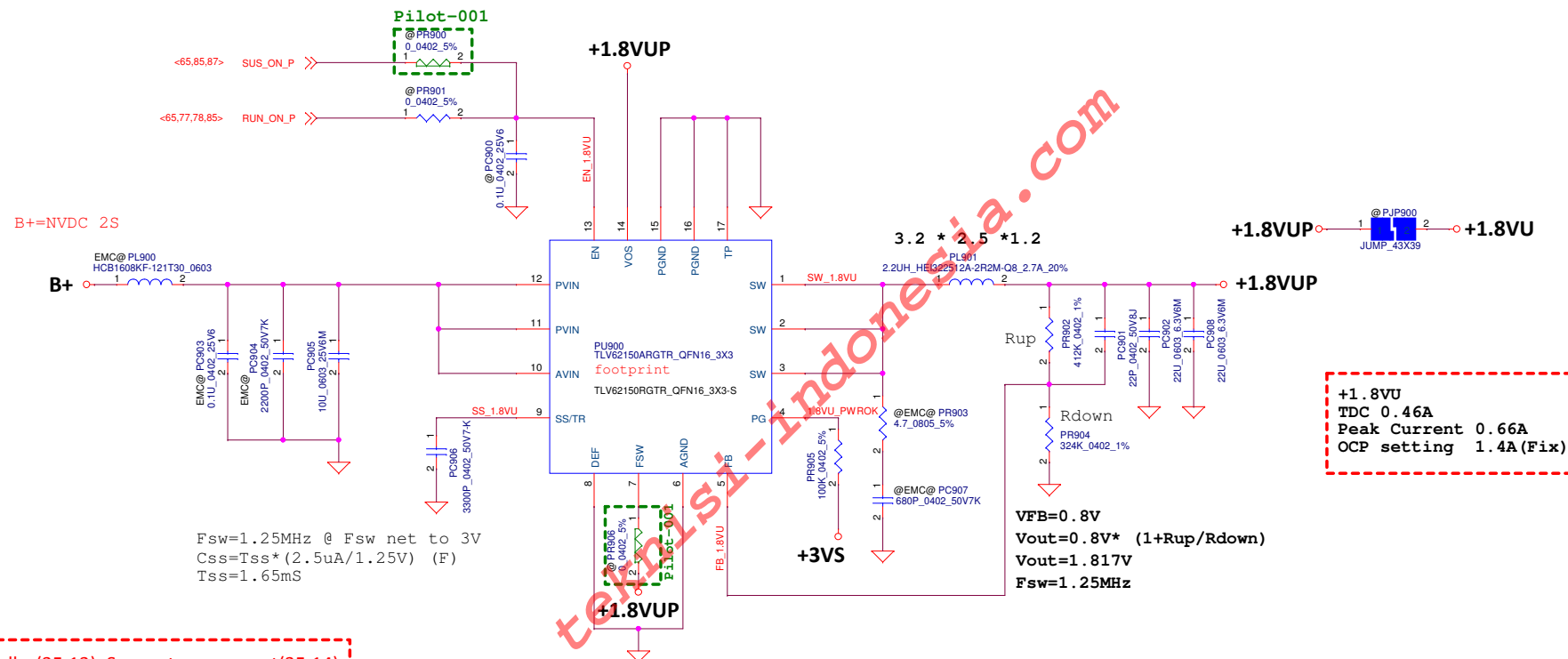
| | | | | |
|----------|----|----|------|-----|
| Mode | S3 | S5 | VOUT | VTT |
| Normal | H | H | on | on |
| Stadby | L | H | on | off |
| Shutdown | L | L | off | off |

Note: S3 - sleep ; S5 - power off

+1.2V_DDR
TDC 4.1A
Peak Current 5.8A
OCP Current 12A

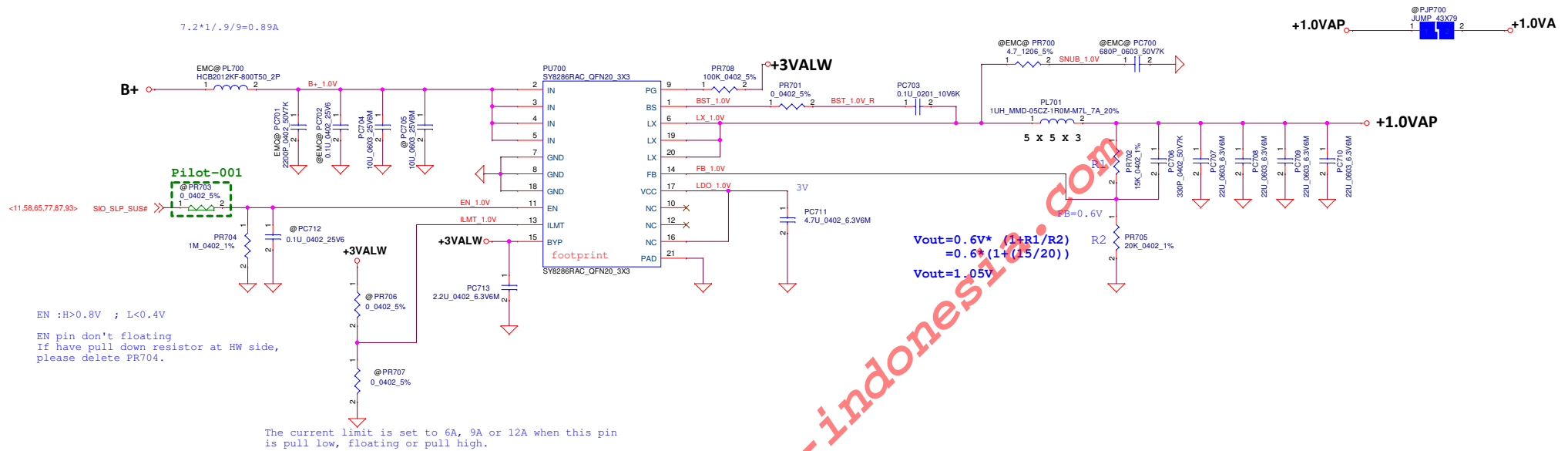
0.6Volt +/- 5%
TDC 0.4A
Peak Current 0.6A
OCP Current 2A (fix)

| | | | | | |
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+1.0VA
TDC 3.5A
Peak Current 5A
OCP current 9A

$$7.2 \times 1 / .9 / 9 = 0.89A$$



| | LPM | VID1 | VID0 | Vout |
|--|-----|------|------|---------|
| | 0 | X | X | 0 (LPM) |
| | 1 | 0 | 0 | 0.85 |
| | 1 | 0 | 1 | 0.875 |
| | 1 | 1 | 0 | 0.95 |
| | 1 | 1 | 1 | 0.975 |

VCCIO
TDC 2.6A
Peak Current 3.7 A
OCP Current 7.6 A Fix by IC
MIN:7A
MAX:8.5A
Frequency:750KHz

| V _{OUT} (V) | R _{MODE} (Ω) |
|----------------------|-----------------------|
| VCCIO | 0 |
| PRIMCORE | Float |
| EDRAM/EOPIO/V1.0A | 100K |
| Others-1.8V/2.5V | 150K |
| Others-3.3V | 150K |

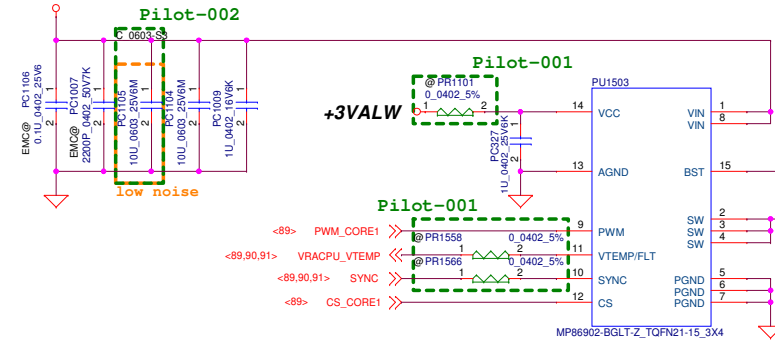
PRIM_CORE
TDC 2.98A
Peak Current 4.26 A
OCP Current 7.6 A Fix by IC
MIN:7A
MAX:8.5A
Choke DCR 34.0mohm

| | LPM | VID1 | VID0 | Vout |
|--|-----|------|------|------------|
| | 0 | X | X | 0.75 (LPM) |
| | 1 | 0 | 0 | 0.9 |
| | 1 | 0 | 1 | 0.95 |
| | 1 | 1 | 0 | 1 |
| | 1 | 1 | 1 | 1.05 |

+1.0VS_VCCIO controller(35.37), Support component(35.38)
+1.0V_PRIM_CORE controller(35.39), Support component(35.40)

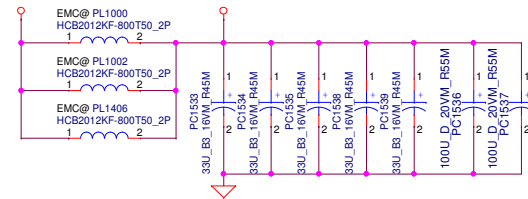
VCC_CORE Dr. MOS (36.2), Support component(36.3)

CPU_B+

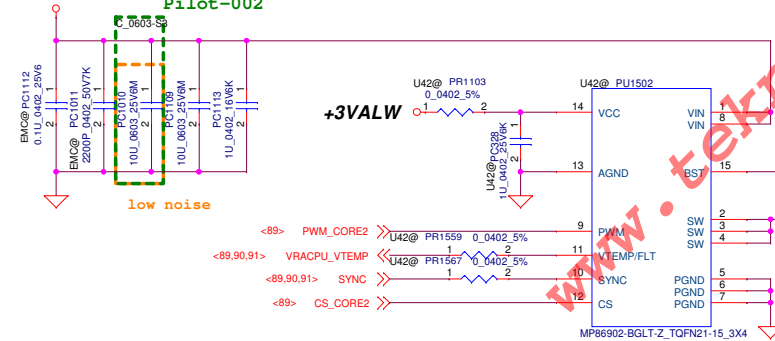


B+

CPU_B+

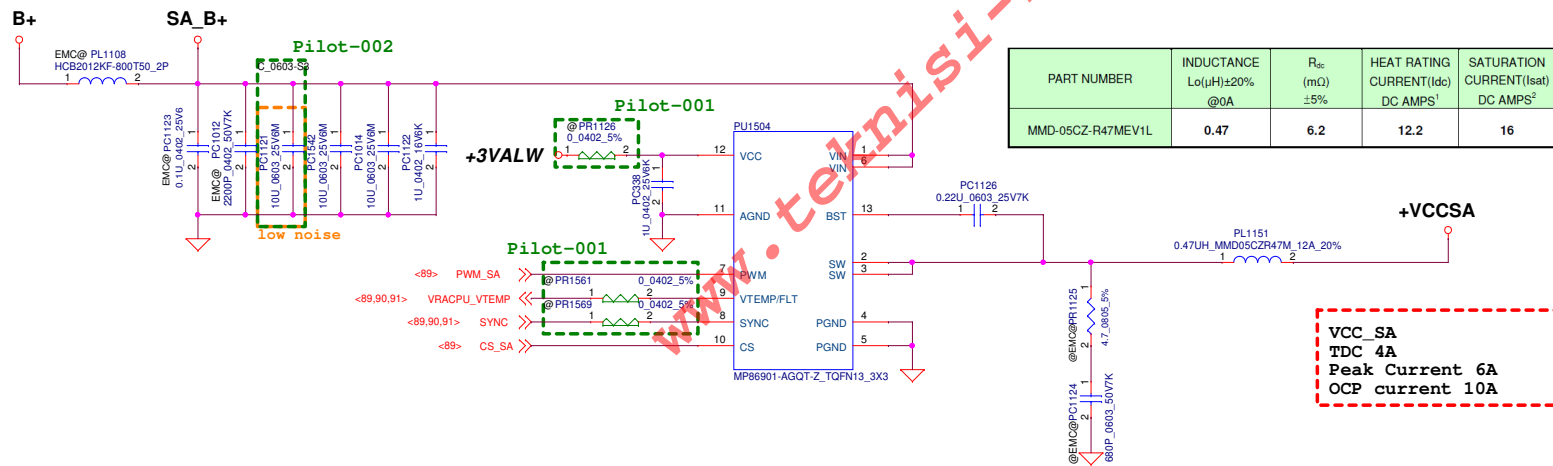
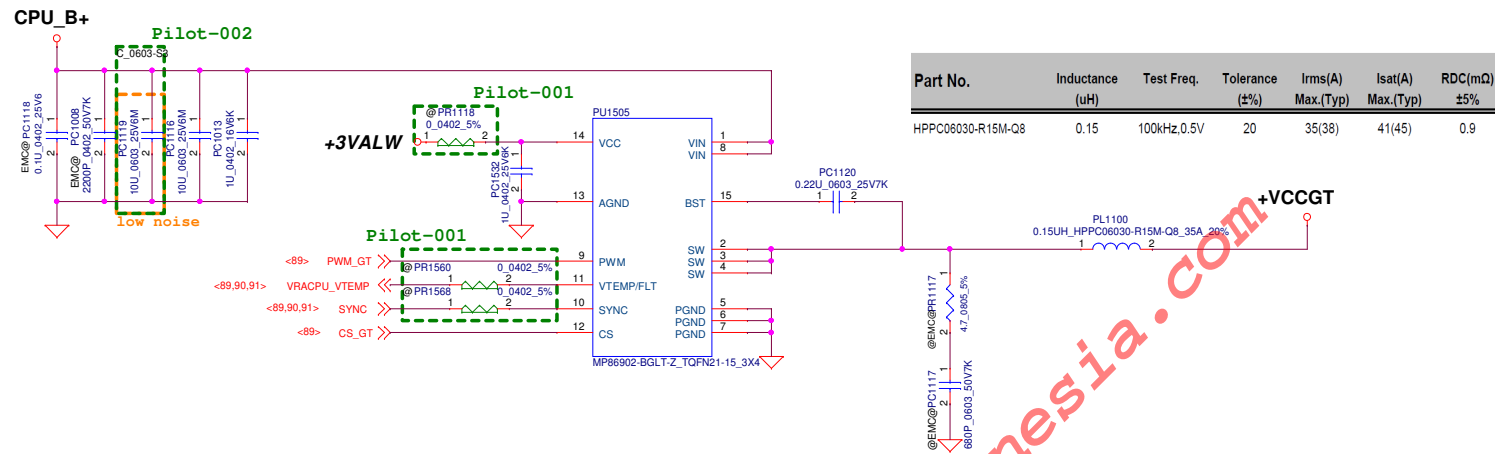


CPU_B+



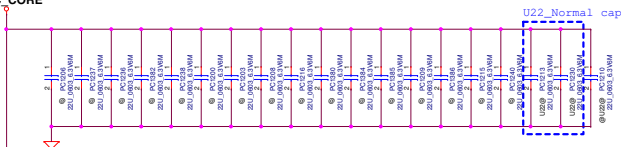
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| | | | | PWR_+VCORE | |
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| | | | | Date | Monday, October 22, 2018 |
| | | | | Sheet | 91 of 100 |
| | | | | Rev | 0.4 |

VCC_GT/SA Dr. MOS (36.2), Support component(36.3)



| | | | | | | |
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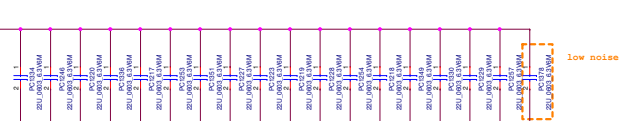
+VCC_CORE



VCC_CORE

U42:22U_0603*23 pcs
U42:22U_0603*27 pcs
U42:330u_B2*4 pcs
U22:330u_B2*2 pcs
U42:1U_0201*54 pcs
U22:1U_0201*54 pcs

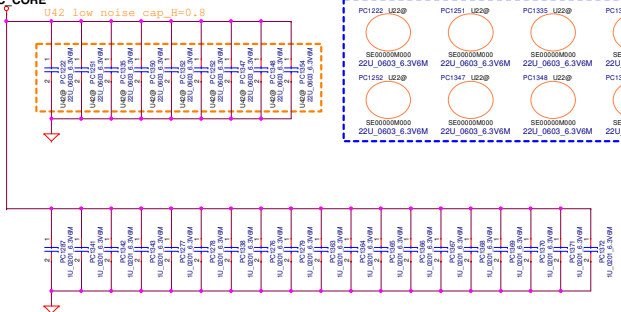
+VCCGT



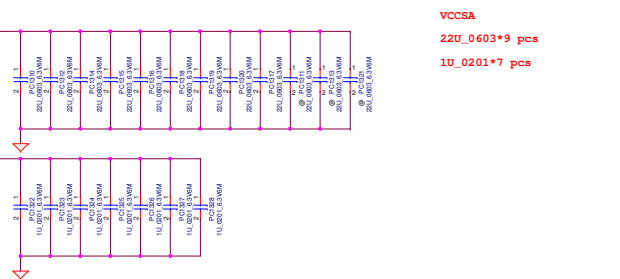
VCCGT

22U_0603*18 pcs
330u_B2*2 pcs
1U_0201*14 pcs

+VCC_CORE



+VCCSA



VCCSA

22U_0603*9 pcs
1U_0201*7 pcs

VCC_CORE output cap(36.4), VCC_GT output cap(36.5), VCC_SA output cap(36.6)

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